دانشگاه سیستان و بلوچستان

الکترونیک ۲- نیمسال دوم ۱۳۹۹

فصل ۷: تقویت کننده های CMOS

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Chapter 7 CMOS Amplifiers

- 7.1 General Considerations
- 7.2 Common-Source Stage
- 7.3 Common-Gate Stage
- 7.4 Source Follower
- 7.5 Summary and Additional Examples

Chapter Outline

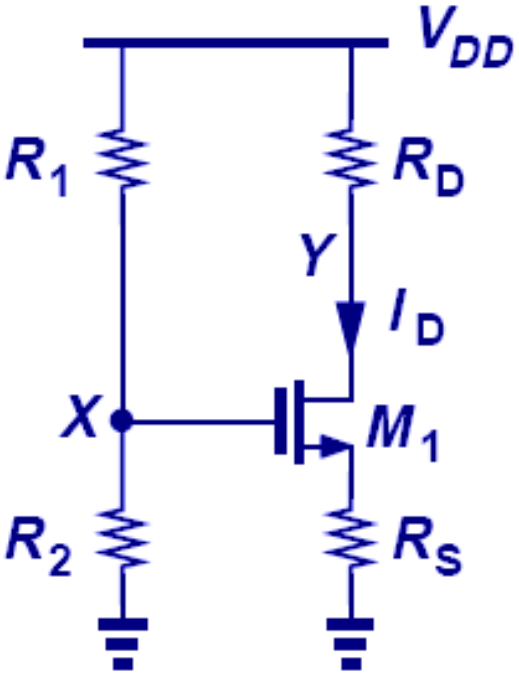
General Concepts

- Biasing of MOS Stages
- Realization of Current Sources

MOS Amplifiers

- Common-Source Stage
- Common-Gate Stage
- Source Follower

MOS Biasing

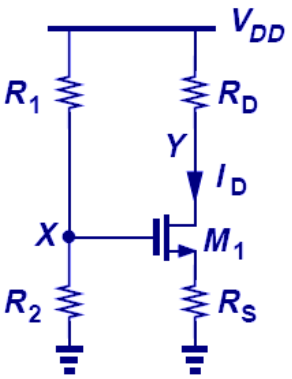


$$V_{GS} = -(V_1 - V_{TH}) + \sqrt{V_1^2 + 2V_1\left(\frac{R_2 V_{DD}}{R_1 + R_2} - V_{TH}\right)}$$

$$V_1 = \frac{1}{\mu_n C_{ox} \frac{W}{L} R_S}$$

- Voltage at X is determined by V_{DD}, R_1, and R_2.
- V_{GS} can be found using the equation above, and I_D can be found by using the NMOS current equation.

MOS Biasing



Since $V_X = V_{GS} + I_D R_S$,

$$\frac{R_2}{R_1 + R_2} V_{DD} = V_{GS} + I_D R_S. \tag{7.2}$$

Also,

$$I_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH})^2. \tag{7.3}$$

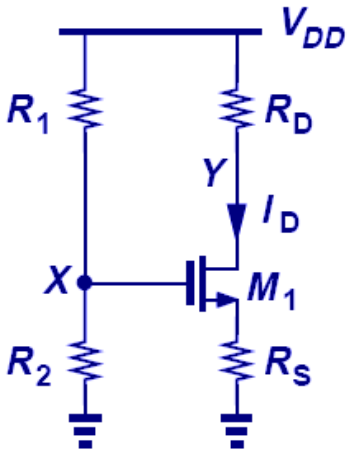
Equations (7.2) and (7.3) can be solved to obtain I_D and V_{GS}, either by iteration or by finding I_D from (7.2) and replacing for it in (7.3):

$$\left(\frac{R_2}{R_1 + R_2} V_{DD} - V_{GS}\right)\frac{1}{R_S} = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH})^2. \tag{7.4}$$

That is

$$V_{GS} = -(V_1 - V_{TH}) + \sqrt{(V_1 - V_{TH})^2 - V_{TH}^2 + \frac{2R_2}{R_1 + R_2} V_1 V_{DD}}, \tag{7.5}$$

MOS Biasing



$$V_{GS} = -(V_1 - V_{TH}) + \sqrt{(V_1 - V_{TH})^2 - V_{TH}^2 + \frac{2R_2}{R_1 + R_2} V_1 V_{DD}}, \tag{7.5}$$

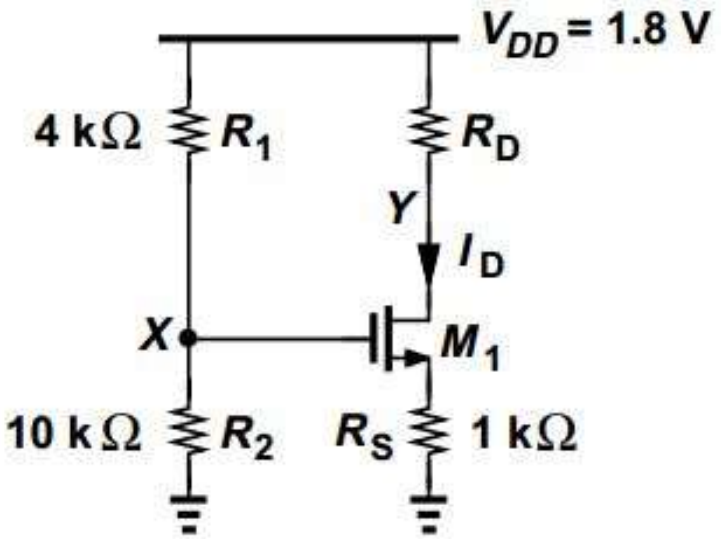
$$= -(V_1 - V_{TH}) + \sqrt{V_1^2 + 2V_1 \left(\frac{R_2 V_{DD}}{R_1 + R_2} - V_{TH} \right)}, \tag{7.6}$$

where

$$V_1 = \frac{1}{\mu_n C_{ox} \frac{W}{L} R_S}. \tag{7.7}$$

This value of V_{GS} can then be substituted in (7.2) to obtain I_D. Of course, V_Y must exceed $V_X - V_{TH}$ to ensure operation in the saturation region.

Example 7.1



Example 7.1

Determine the bias current of M_1 in Fig. 7.1

assuming $V_{TH} = 0.5$ V, $\mu_n C_{ox} = 100\ \mu\text{A/V}^2$, $W/L = 5/0.18$, and $\lambda = 0$.

What is the maximum allowable value of R_D for M_1 to remain in saturation?

Solution Example 7.1

$$V_X = \frac{R_2}{R_1 + R_2} V_{DD}$$
$$= 1.286 \text{ V}.$$

With an initial guess $V_{GS} = 1$ V, the voltage drop across R_S can be expressed as $V_X - V_{GS} = 286$ mV, yielding a drain current of 286 μA. Substituting for I_D in Eq. (7.3) gives the new value of V_{GS} as

$$V_{GS} = V_{TH} + \sqrt{\frac{2I_D}{\mu_n C_{ox} \frac{W}{L}}} \tag{7.10}$$

$$= 0.954 \text{ V}. \tag{7.11}$$

Consequently,

$$I_D = \frac{V_X - V_{GS}}{R_S} \tag{7.12}$$

$$= 332 \ \mu\text{A}, \tag{7.13}$$

and hence

$$V_{GS} = 0.989 \text{ V}. \tag{7.14}$$

This gives $I_D = 297$ μA.

Solution Example 7.1

As seen from the iterations, the solutions converge more slowly than those encountered in Chapter 5 for bipolar circuits. This is due to the quadratic (rather than exponential) I_D-V_{GS} dependence. We may therefore utilize the exact result in (7.6) to avoid lengthy calculations. Since $V_1 = 0.36$ V,

$$V_{GS} = 0.974 \text{ V} \tag{7.15}$$

and

$$I_D = \frac{V_X - V_{GS}}{R_S} \tag{7.16}$$

$$= 312\ \mu\text{A}. \tag{7.17}$$

The maximum allowable value of R_D is obtained if $V_Y = V_X - V_{TH} = 0.786$ V. That is,

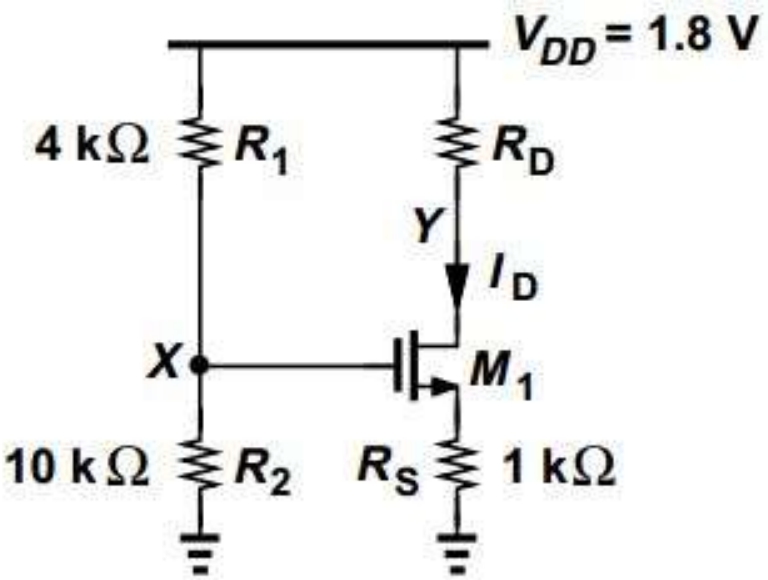
$$R_D = \frac{V_{DD} - V_Y}{I_D} \tag{7.18}$$

$$= 3.25\ \text{k}\Omega. \tag{7.19}$$

Example 7.2

Example 7.2

In the circuit of Example 7.1, assume M_1 is in saturation and $R_D = 2.5\ \text{k}\Omega$ and compute (a) the maximum allowable value of W/L and (b) the minimum allowable value of R_S (with $W/L = 5/0.18$). Assume $\lambda = 0$.



Solution Example 7.2

Solution

(a) As W/L becomes larger, M_1 can carry a larger current for a given V_{GS}. With $R_D = 2.5\ \text{k}\Omega$ and $V_X = 1.286$ V, the maximum allowable value of I_D is given by

$$I_D = \frac{V_{DD} - V_Y}{R_D} \tag{7.20}$$

$$= 406\ \mu\text{A}. \tag{7.21}$$

The voltage drop across R_S is then equal to 406 mV, yielding $V_{GS} = 1.286\ \text{V} - 0.406\ \text{V} = 0.88$ V. In other words, M_1 must carry a current of 406 μA with $V_{GS} = 0.88$ V:

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2 \tag{7.22}$$

$$406\ \mu\text{A} = (50\ \mu\text{A/V}^2)\frac{W}{L}(0.38\ \text{V})^2; \tag{7.23}$$

thus,

$$\frac{W}{L} = 56.2. \tag{7.24}$$

Solution Example 7.2

(b) With $W/L = 5/0.18$, the minimum allowable value of R_S gives a drain current of 406 μA. Since

$$V_{GS} = V_{TH} + \sqrt{\frac{2I_D}{\mu_n C_{ox}\frac{W}{L}}} \tag{7.25}$$

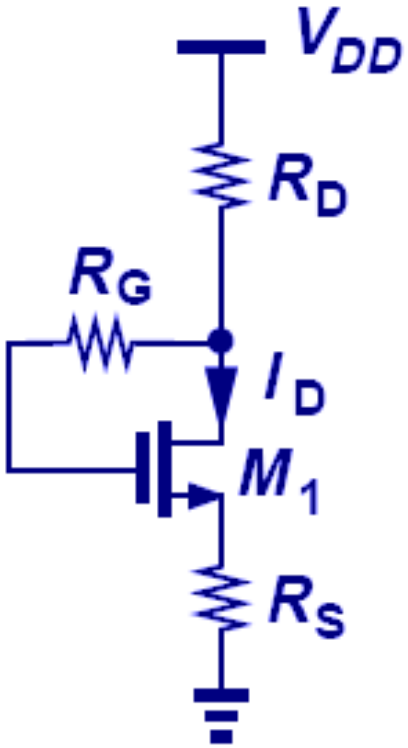
$$= 1.041\,\text{V}, \tag{7.26}$$

the voltage drop across R_S is equal to $V_X - V_{GS} = 245$ mV. It follows that

$$R_S = \frac{V_X - V_{GS}}{I_D} \tag{7.27}$$

$$= 604\,\Omega. \tag{7.28}$$

Self-Biased MOS Stage

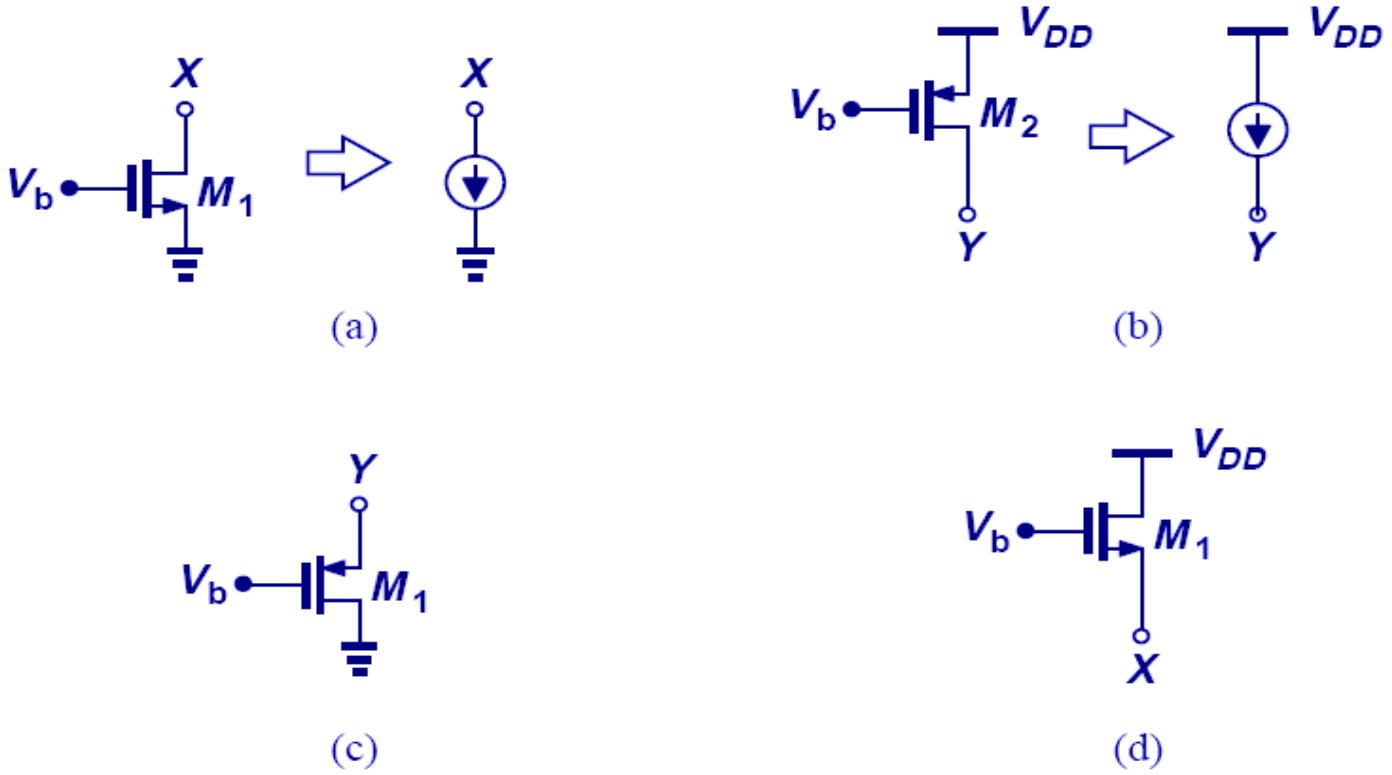


$$I_D R_D + V_{GS} + R_S I_D = V_{DD}$$

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}[V_{DD} - (R_S + R_D)I_D - V_{TH}]^2,$$

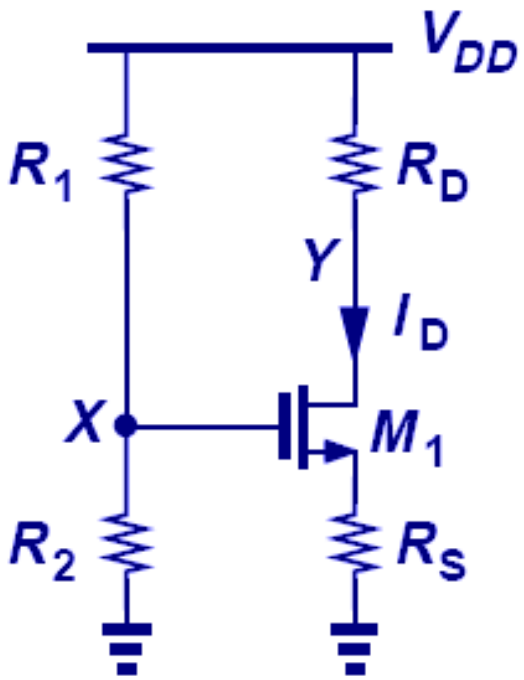
- **The circuit above is analyzed by noting M1 is in saturation and no potential drop appears across R_G.**

Current Sources



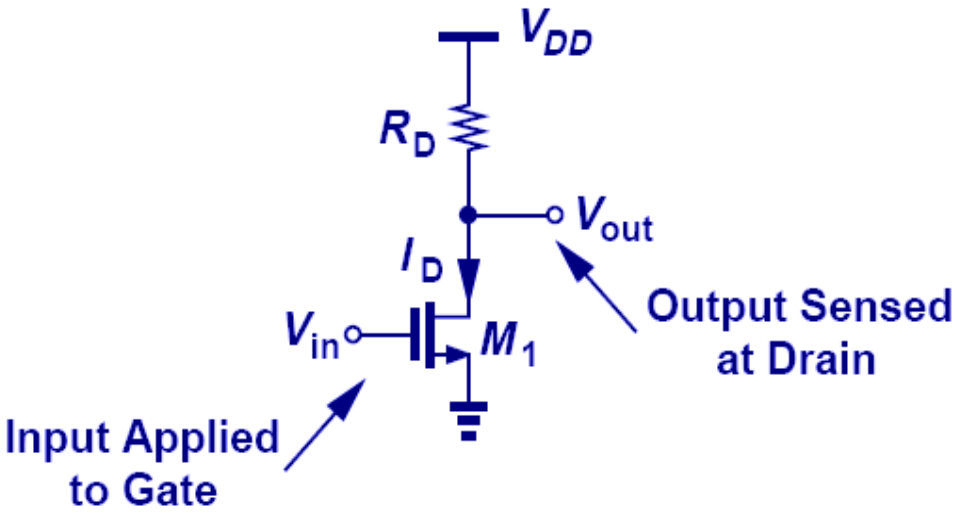
- When in saturation region, a MOSFET behaves as a current source.
- NMOS draws current from a point to ground (sinks current), whereas PMOS draws current from V_{DD} to a point (sources current).

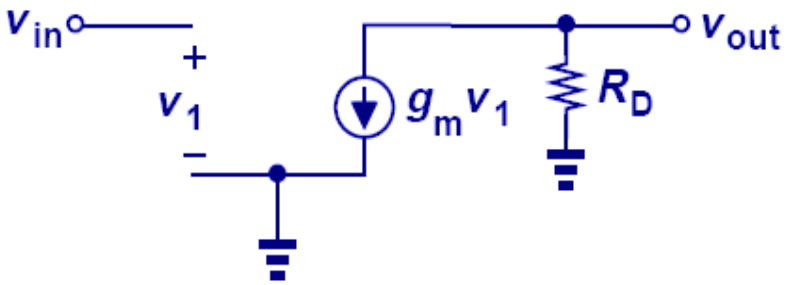
آرایش تقویت کننده؟



- سورس مشترک (CS)
- درین مشترک (دنبال کننده سورس) (CD)
- گیت مشترک (CG)

Common-Source Stage



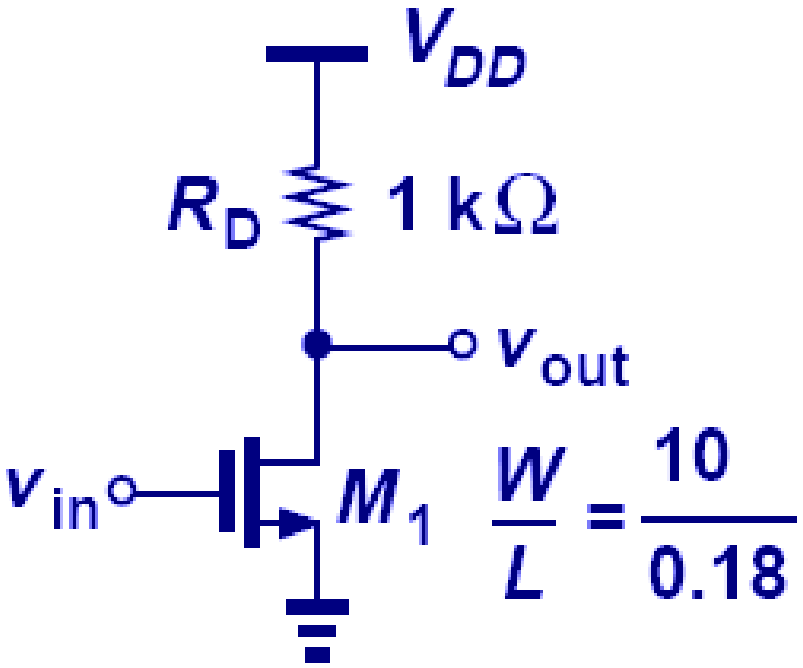


$$\lambda = 0$$

$$A_v = -g_m R_D$$

$$A_v = -\sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} R_D$$

Example 7.4: Operation in Saturation



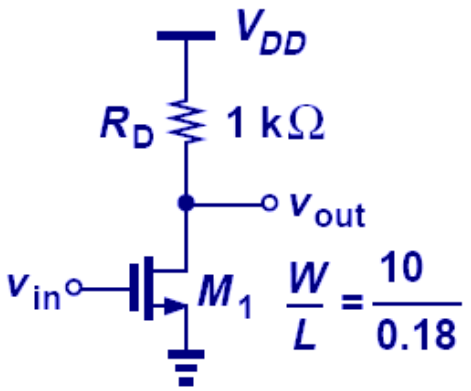
$$R_D I_D < V_{DD} - (V_{GS} - V_{TH})$$

- In order to maintain operation in saturation, V_{out} cannot fall below V_{in} by more than one threshold voltage.
- The condition above ensures operation in saturation.

Example 7.4

Solution

$$g_m = \sqrt{2\mu_n C_{ox}\frac{W}{L}I_D}$$
$$= \frac{1}{300\,\Omega}.$$

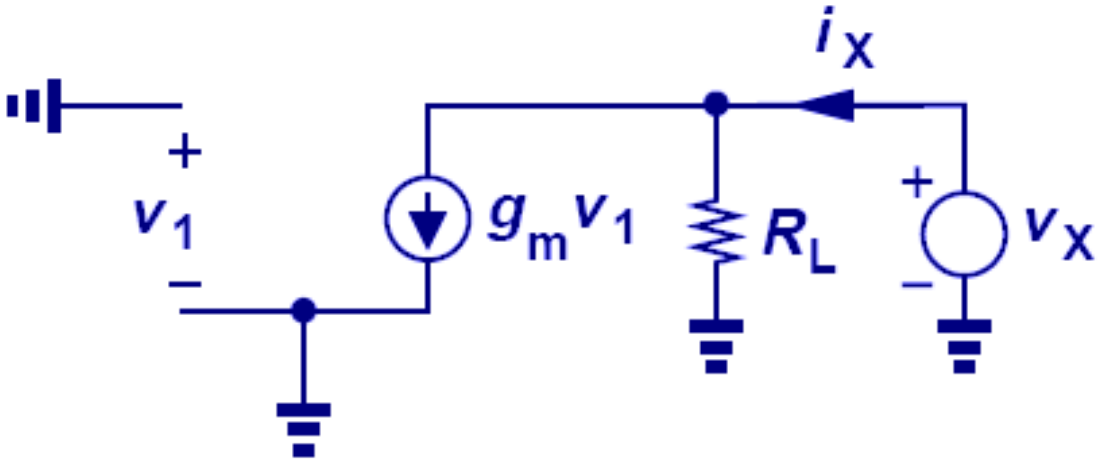


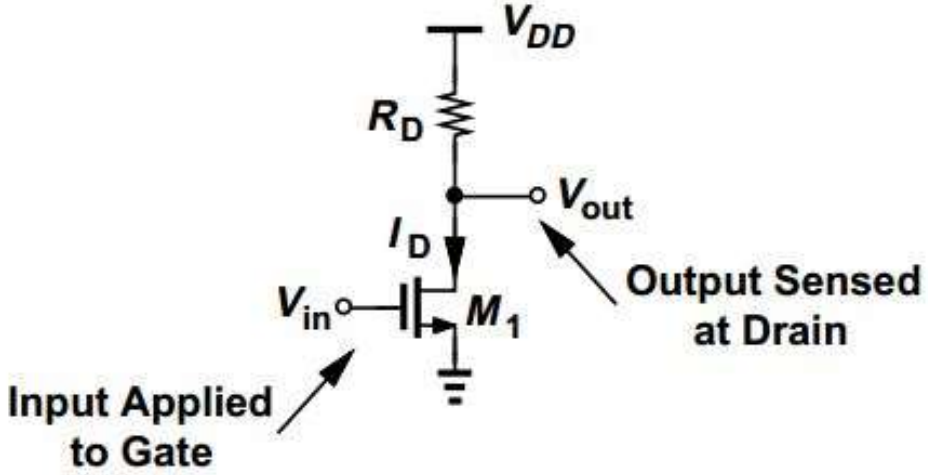
$$A_v = -g_m R_D$$
$$= 3.33.$$

$$V_{GS} = V_{TH} + \sqrt{\frac{2I_D}{\mu_n C_{ox}\frac{W}{L}}}$$
$$= 1.1\ \text{V}.$$

The drain voltage is equal to $V_{DD} - R_D I_D = 0.8$ V. Since $V_{GS} - V_{TH} = 0.6$ V, the device indeed operates in saturation and has a margin of 0.2 V with respect to the triode region. For example, if R_D is doubled with the intention of doubling A_v, then M_1 enters the triode region and its transconductance drops.

CS Stage with λ=0



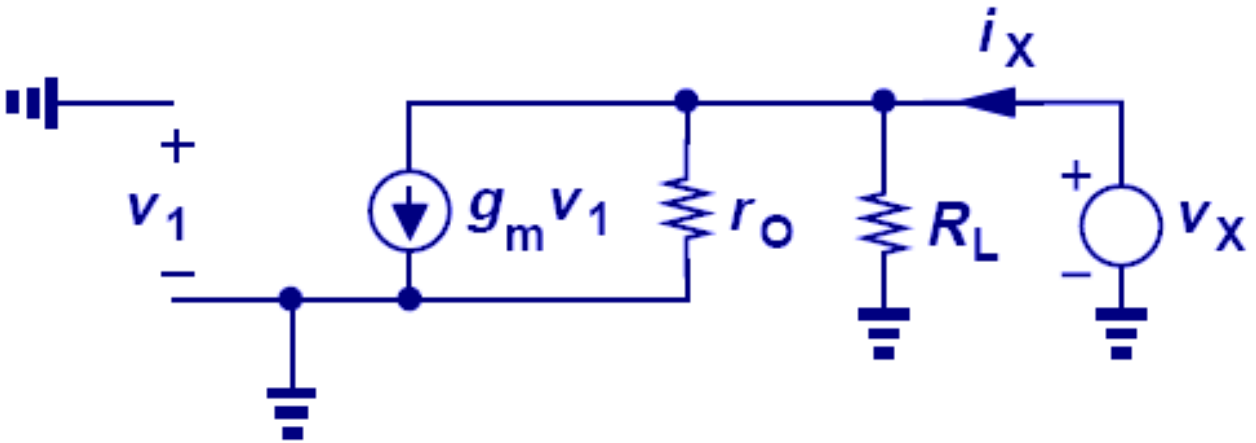


$$A_v = -g_m R_L$$

$$R_{in} = \infty$$

$$R_{out} = R_L$$

CS Stage with $\lambda \neq 0$



$$A_v = -g_m\left(R_L \parallel r_O\right)$$

$$R_{in} = \infty$$

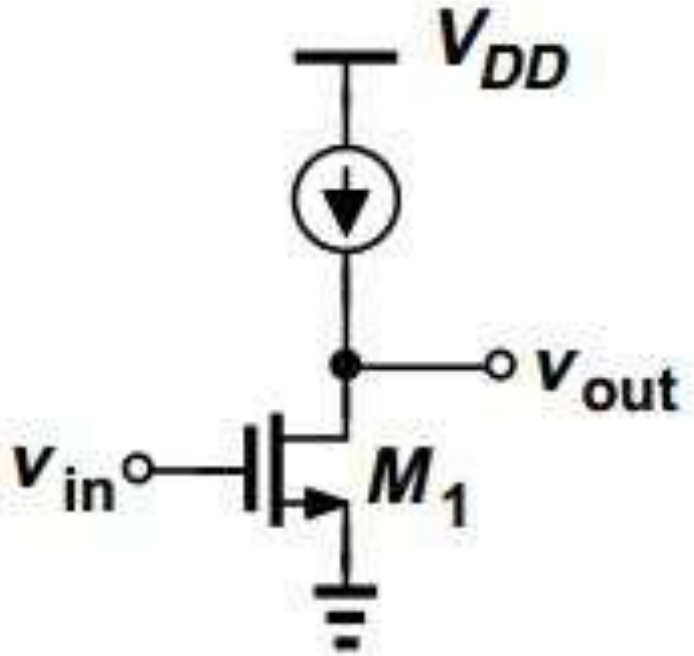
$$R_{out} = R_L \parallel r_O$$

- **However, Early effect and channel length modulation affect CE and CS stages in a similar manner.**

Example 7.5: CS Gain Variation with Channel Length

Example 7.5

Assuming M_1 operates in saturation, determine the voltage gain of the circuit depicted in Fig. 7.9(a) and plot the result as a function of the transistor channel length while other parameters remain constant.



Example 7.5: CS Gain Variation with Channel Length

Solution

The ideal current source presents an infinite small-signal resistance, allowing the use of (7.46) with $R_D = \infty$:

$$A_v = -g_m r_O. \tag{7.49}$$

This is the highest voltage gain that a single transistor can provide. Writing $g_m = \sqrt{2\mu_n C_{ox}(W/L)I_D}$ and $r_O = (\lambda I_D)^{-1}$, we have

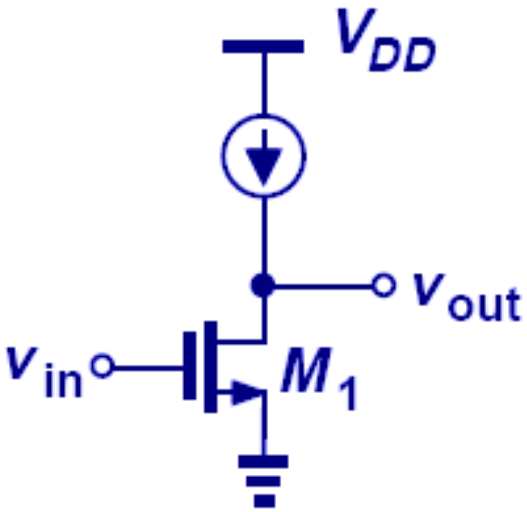
$$|A_v| = \frac{\sqrt{2\mu_n C_{ox}\dfrac{W}{L}}}{\lambda\sqrt{I_D}}. \tag{7.50}$$

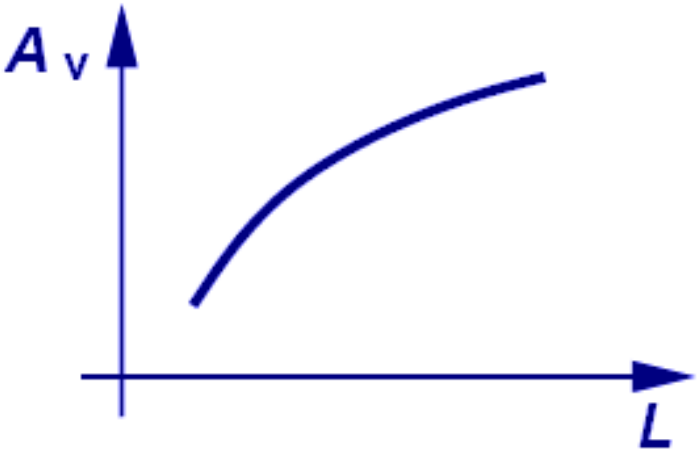
This result may imply that $|A_v|$ falls as L increases, but recall from Chapter 6 that $\lambda \propto L^{-1}$:

$$|A_v| \propto \sqrt{\frac{2\mu_n C_{ox} W L}{I_D}}. \tag{7.51}$$

Consequently, $|A_v|$ increases with L [Fig. 7.9(b)].

Example 7.5: CS Gain Variation with Channel Length

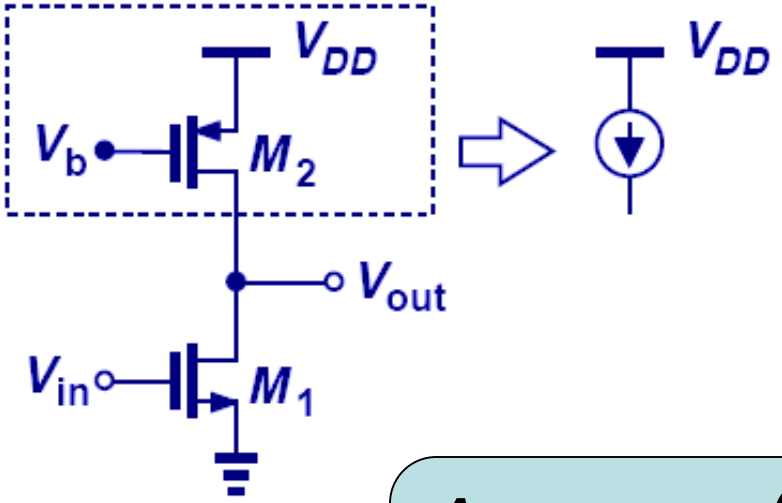


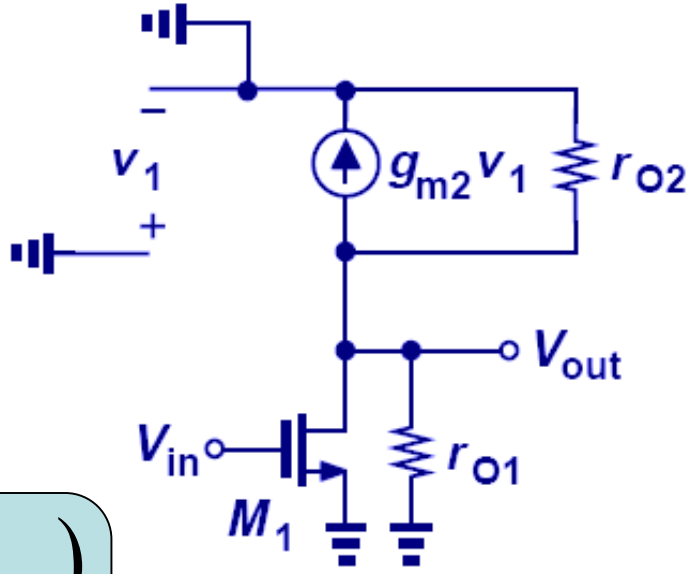


$$|A_v| = \frac{\sqrt{2\mu_n C_{ox}\frac{W}{L}}}{\lambda\sqrt{I_D}} \propto \sqrt{\frac{2\mu_n C_{ox} WL}{I_D}}$$

- **Since λ is inversely proportional to L, the voltage gain actually becomes proportional to the square root of L.**

CS Stage with Current-Source Load



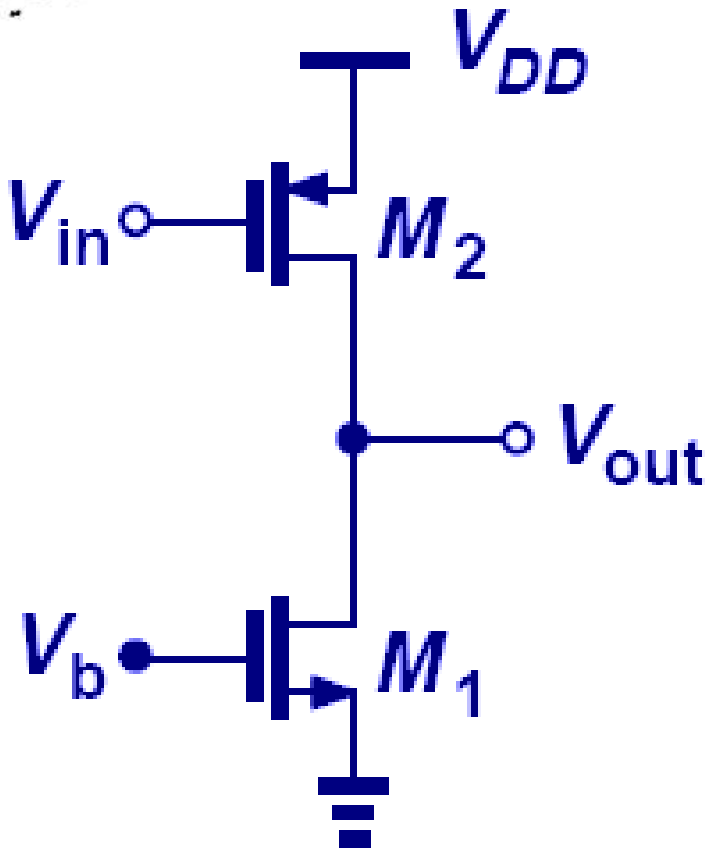


$$A_v = -g_{m1}(r_{O1} \parallel r_{O2})$$

$$R_{out} = r_{O1} \parallel r_{O2}$$

- To alleviate the headroom problem, an active current-source load is used.
- This is advantageous because a current-source has a high output resistance and can tolerate a small voltage drop across it.

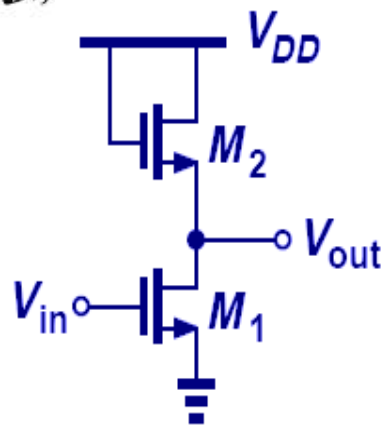
PMOS CS Stage with NMOS as Load

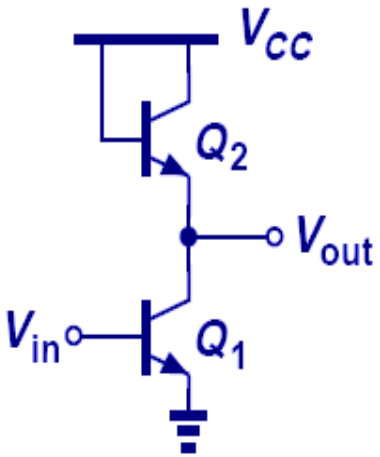


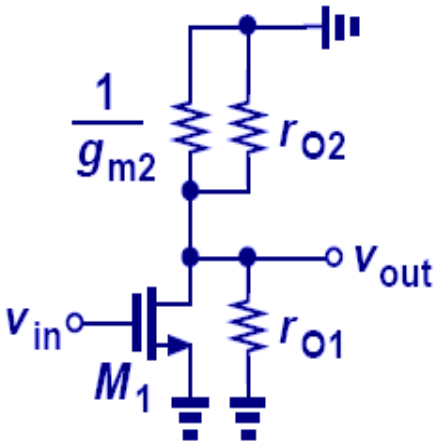
$$A_v = -g_{m2}(r_{O1} \| r_{O2})$$

- **Similarly, with PMOS as input stage and NMOS as the load, the voltage gain is the same as before.**

CS Stage with Diode-Connected Load



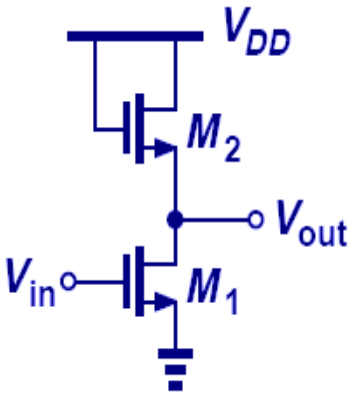


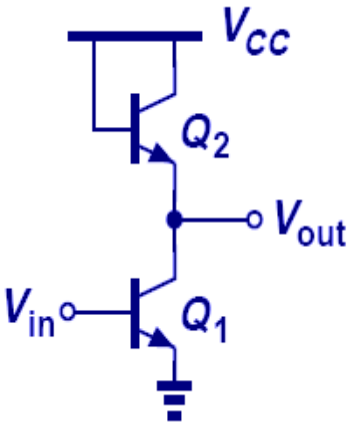


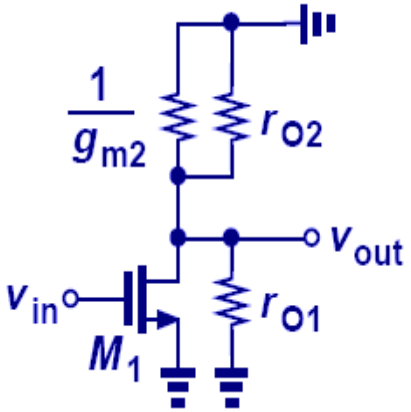
$$A_v = -g_{m1}\left(\frac{1}{g_{m2}} || r_{O2} || r_{O1}\right)$$

$$\begin{aligned} A_v &= -g_{m1} \cdot \frac{1}{g_{m2}} \\ &= -\frac{\sqrt{2\mu_n C_{ox}(W/L)_1 I_D}}{\sqrt{2\mu_n C_{ox}(W/L)_2 I_D}} \\ &= -\sqrt{\frac{(W/L)_1}{(W/L)_2}}. \end{aligned}$$

CS Stage with Diode-Connected Load





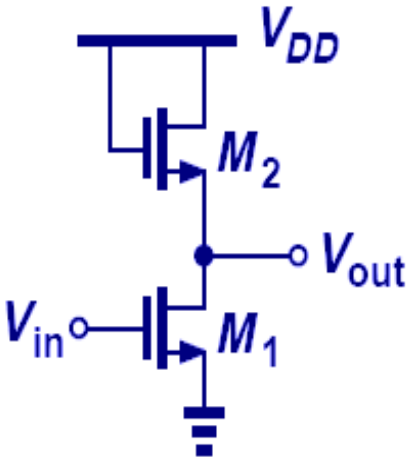


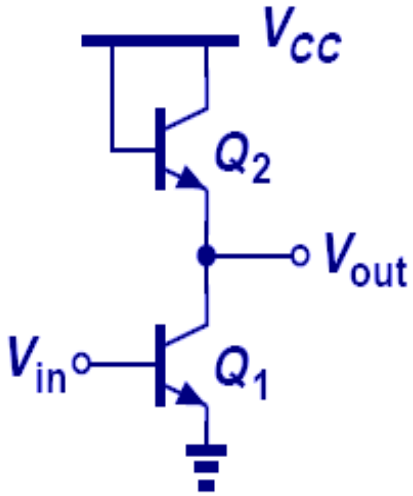
$$A_v = -g_{m1}\left(\frac{1}{g_{m2}}||r_{O2}||r_{O1}\right)$$

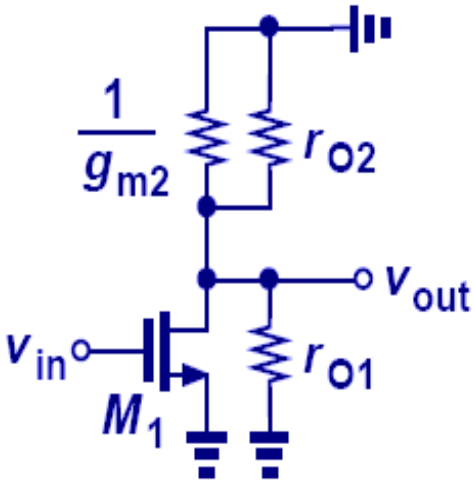
$$R_{out} = \frac{1}{g_{m2}}||r_{O2}||r_{O1}$$

$$\begin{aligned} A_v &= -g_{m1}\cdot\frac{1}{g_{m2}} \\ &= -\frac{I_{C1}}{V_T}\cdot\frac{1}{I_{C2}/V_T} \\ &\approx -1. \end{aligned}$$

CS Stage with Diode-Connected Load





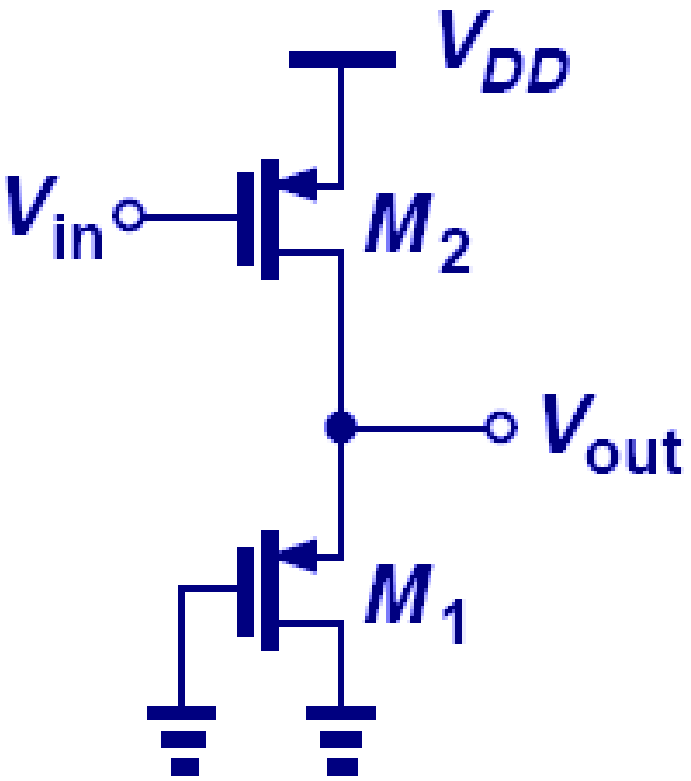


$$A_v = -g_{m1} \cdot \frac{1}{g_{m2}} = -\sqrt{\frac{(W/L)_1}{(W/L)_2}}$$

$$A_v = -g_{m1}\left(\frac{1}{g_{m2}} \parallel r_{O2} \parallel r_{O1}\right)$$

- **Lower gain, but less dependent on process parameters.**

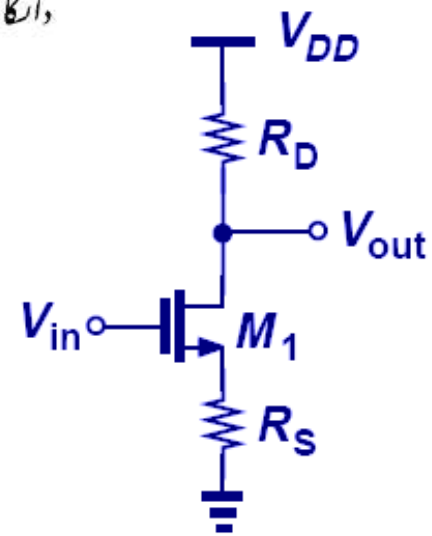
CS Stage with Diode-Connected PMOS Device

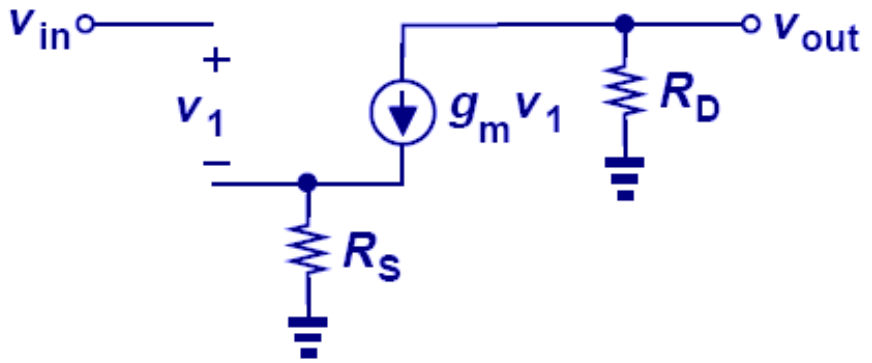


$$A_v = -g_{m2}\left(\frac{1}{g_{m1}} \parallel r_{o1} \parallel r_{o2}\right)$$

- **Note that PMOS circuit symbol is usually drawn with the source on top of the drain.**

CS Stage with Degeneration





$$v_{in} = v_1 + g_m v_1 R_S$$

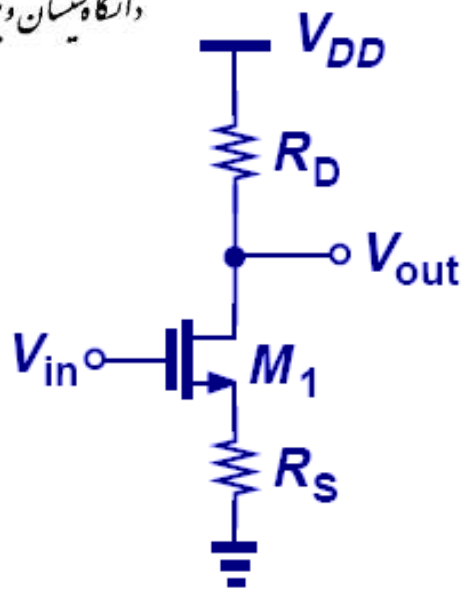
$$v_1 = \frac{v_{in}}{1 + g_m R_S}.$$

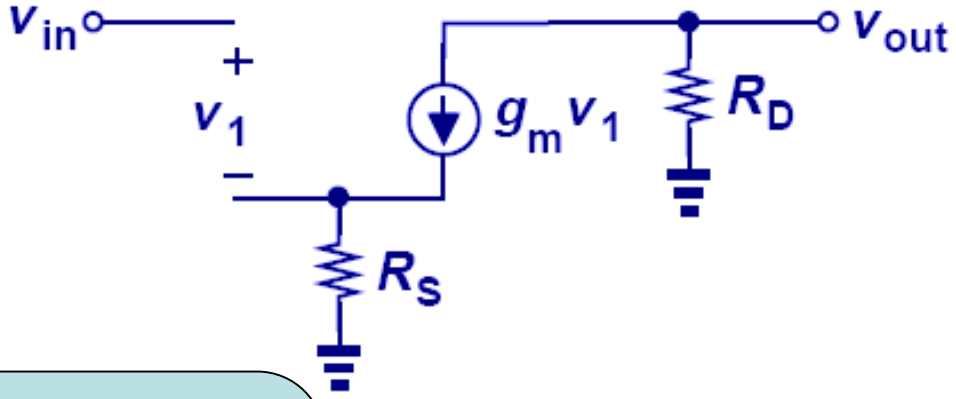
$v_{out} = -g_m v_1 R_D$ and

$$\frac{v_{out}}{v_{in}} = -\frac{g_m R_D}{1 + g_m R_S}$$

$$= -\frac{R_D}{\frac{1}{g_m} + R_S},$$

CS Stage with Degeneration



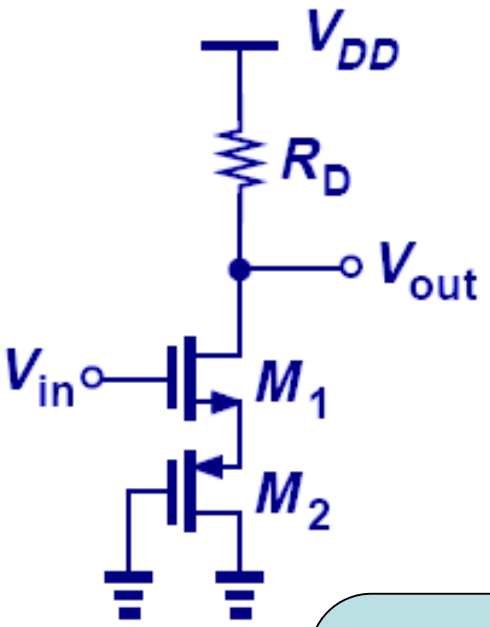


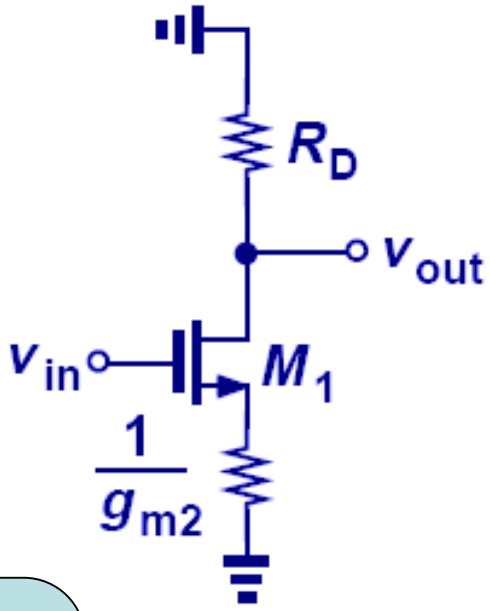
$$A_v = -\frac{R_D}{\frac{1}{g_m} + R_S}$$

$$\lambda = 0$$

- **Similar to bipolar counterpart, when a CS stage is degenerated, its gain, I/O impedances, and linearity change.**

Example7.8: CS Stage with Degeneration

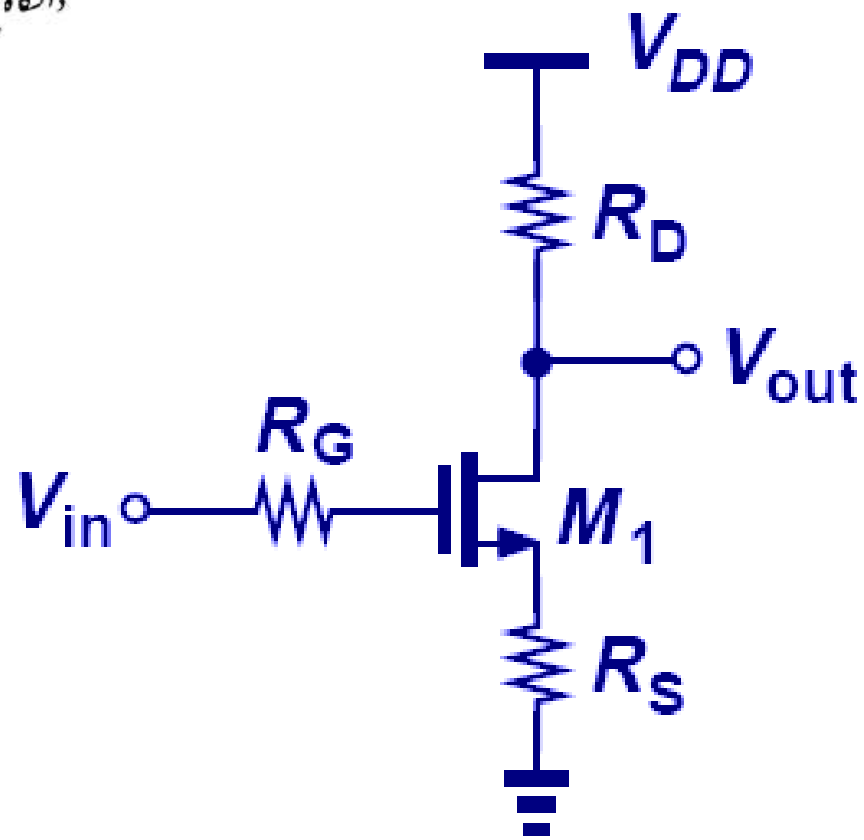




$$A_v = -\frac{R_D}{\frac{1}{g_{m1}} + \frac{1}{g_{m2}}}$$

- **A diode-connected device degenerates a CS stage.**

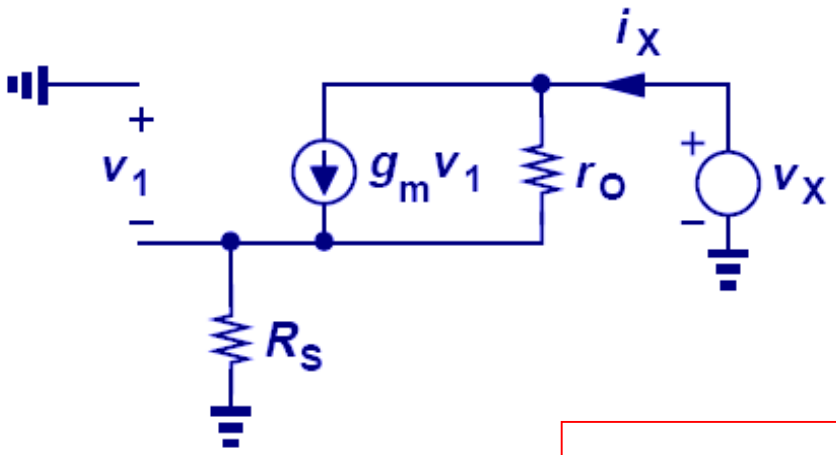
CS Stage with Gate Resistance



$$V_{R_G} = 0$$

- **Since at low frequencies, the gate conducts no current, gate resistance does not affect the gain or I/O impedances.**

Output Impedance of CS Stage with Degeneration



$$v_1 = -i_X R_S.$$

$$i_X - g_m v_1 =$$

$$i_X - g_m(-i_X R_S) = i_X + g_m i_X R_S.$$

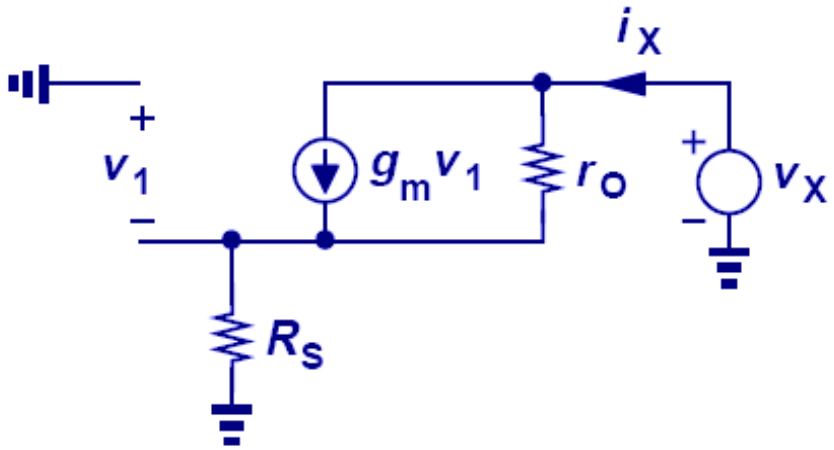
$$r_O(i_X + g_m i_X R_S) + i_X R_S = v_X,$$

$$\frac{v_X}{i_X} = r_O(1 + g_m R_S) + R_S$$

$$= (1 + g_m r_O)R_S + r_O$$

$$\approx g_m r_O R_S + r_O.$$

Output Impedance of CS Stage with Degeneration



$$r_O(i_X + g_m i_X R_S) + i_X R_S = v_X,$$

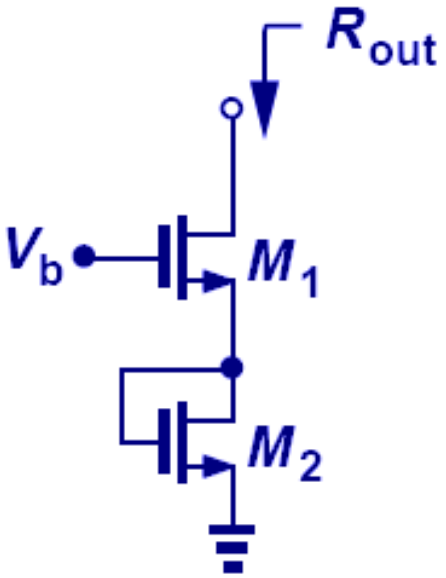
$$\frac{v_X}{i_X} = r_O(1 + g_m R_S) + R_S$$

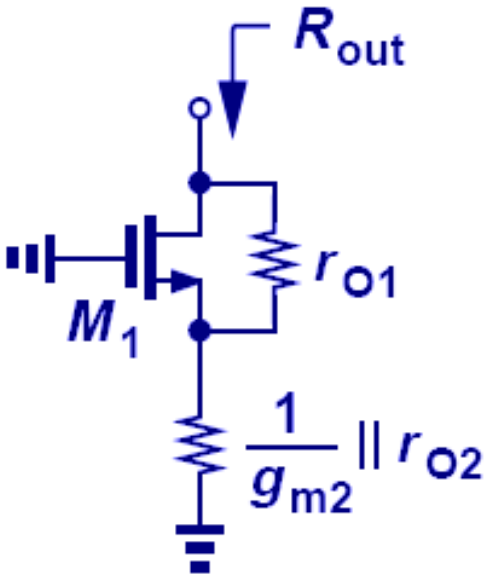
$$= (1 + g_m r_O)R_S + r_O$$

$$\approx g_m r_O R_S + r_O.$$

$$r_{out} \approx g_m r_O R_S + r_O$$

Example 7.9: Output Impedance Example (I)





$$(1/g_{m2})||r_{O2} \approx 1/g_{m2}.$$

$$R_{out} = r_{O1}\left(1 + g_{m1}\frac{1}{g_{m2}}\right) + \frac{1}{g_{m2}}$$

- When $1/g_m$ is parallel with r_{O2}, we often just consider $1/g_m$.

Example 7.9

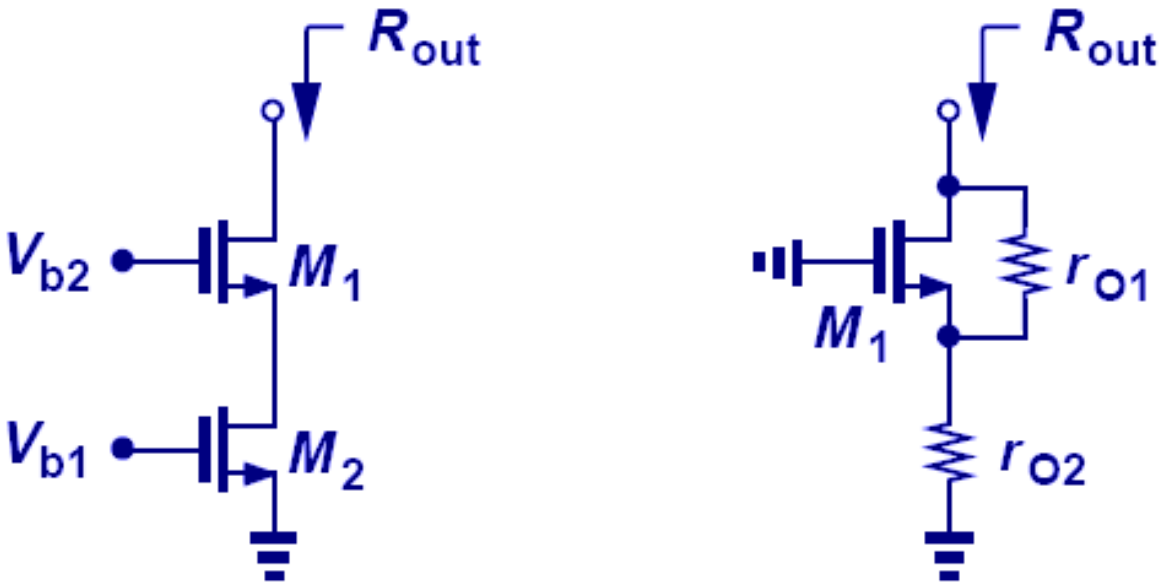
$$(1/g_{m2})||r_{O2} \approx 1/g_{m2}.$$

$$R_{out} = r_{O1}\left(1 + g_{m1}\frac{1}{g_{m2}}\right) + \frac{1}{g_{m2}}$$

since $g_{m1} = g_{m2} = g_m$,

$$R_{out} = 2r_{O1} + \frac{1}{g_m}$$
$$\approx 2r_{O1}.$$

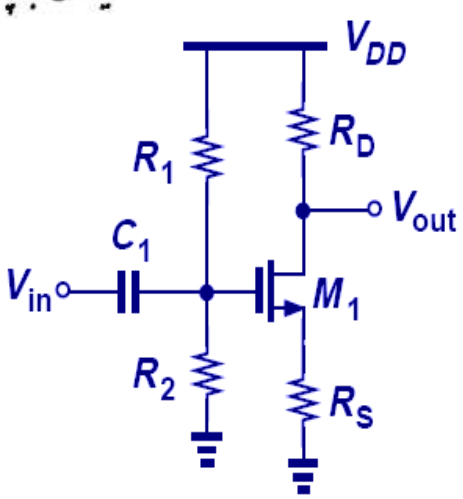
Example 7.10: Output Impedance Example (II)

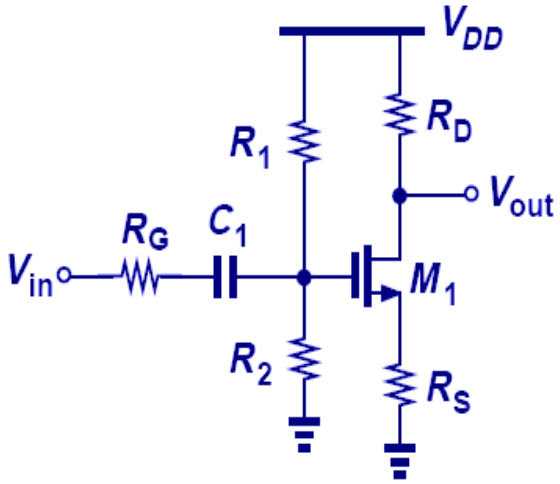


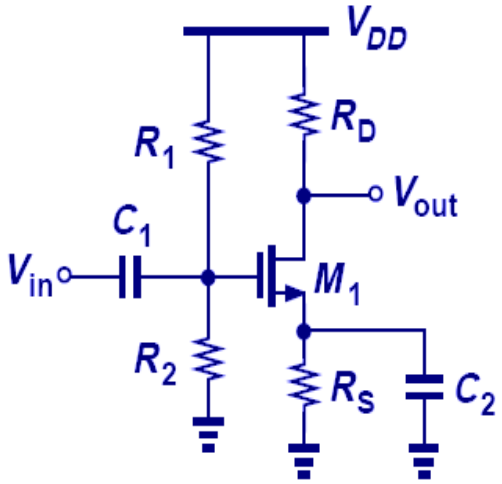
$$R_{out} = (1 + g_{m1} r_{O1}) r_{O2} + r_{O1}$$
$$\approx g_{m1} r_{O1} r_{O2} + r_{O1}.$$

$$R_{out} \approx g_{m1} r_{O1} r_{O2} + r_{O1}$$

CS Core with Biasing







$$A_v = \frac{R_1 \| R_2}{R_G + R_1 \| R_2} \cdot \frac{-R_D}{\frac{1}{g_m} + R_S}, A_v = -\frac{R_1 \| R_2}{R_G + R_1 \| R_2} g_m R_D$$

- **Degeneration is used to stabilize bias point, and a bypass capacitor can be used to obtain a larger small-signal voltage gain at the frequency of interest.**

دانشگاه سیستان و بلوچستان

الکترونیک ۲- نیمسال اول ۱۳۹۹

فصل ۷: قسمت دوم تقویت کننده های CMOS

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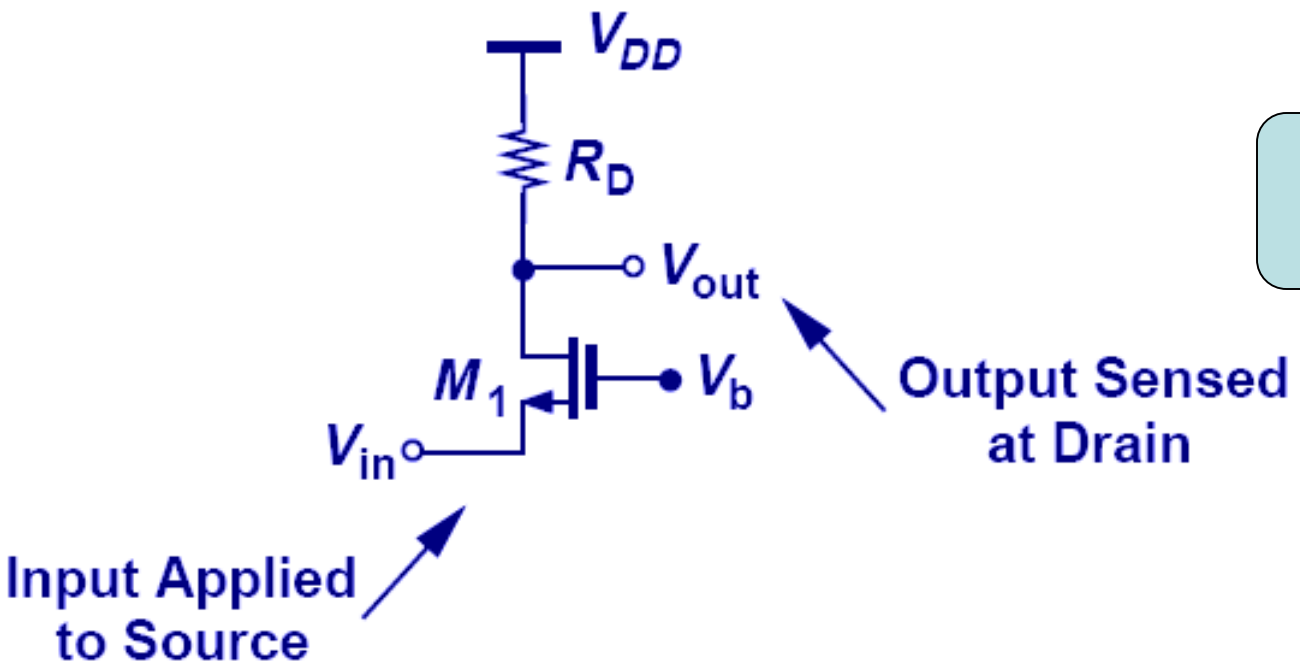
mamansouri@yahoo.com

Chapter 7 (part 2) CMOS Amplifiers

- 7.3 Common-Gate Stage
- 7.4 Source Follower
- 7.5 Summary and Additional Examples

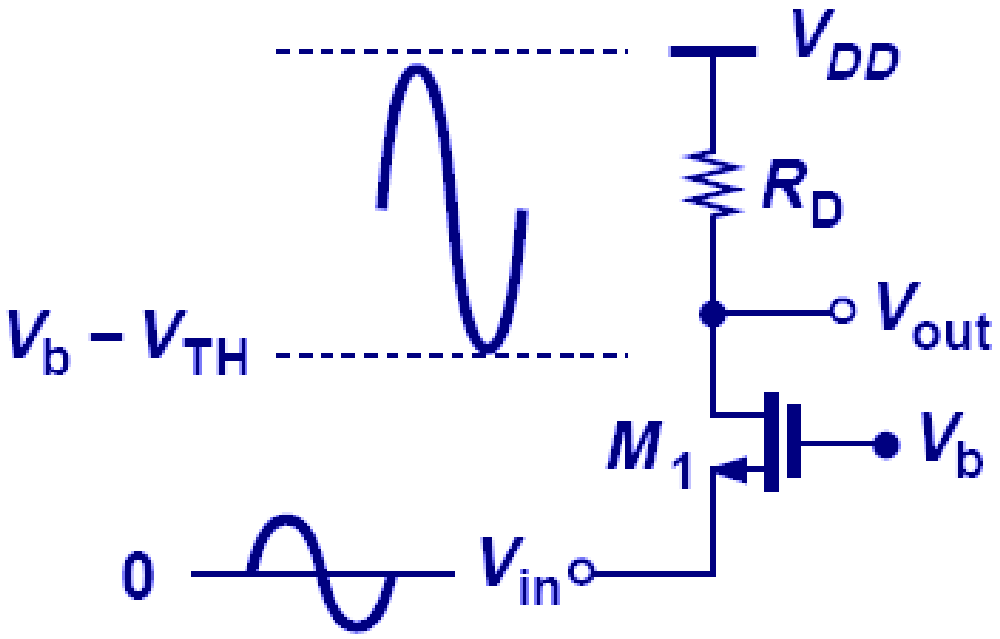
Common-Gate Stage



$$A_v = g_m R_D$$

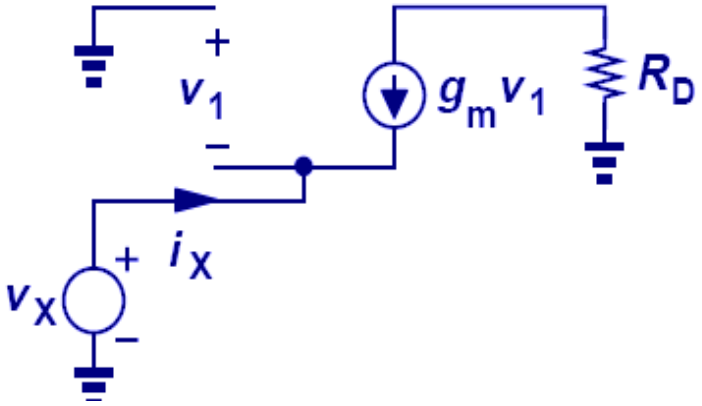
- **Common-gate stage is similar to common-base stage: a rise in input causes a rise in output. So the gain is positive.**

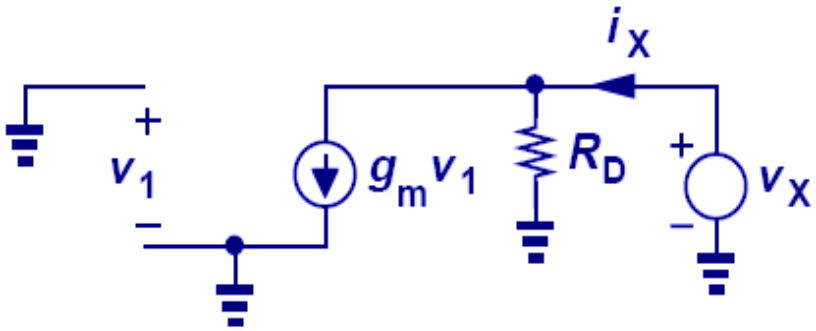
Signal Levels in CG Stage



- In order to maintain M_1 in saturation, the signal swing at V_{out} cannot fall below V_b-V_{TH}.

I/O Impedances of CG Stage





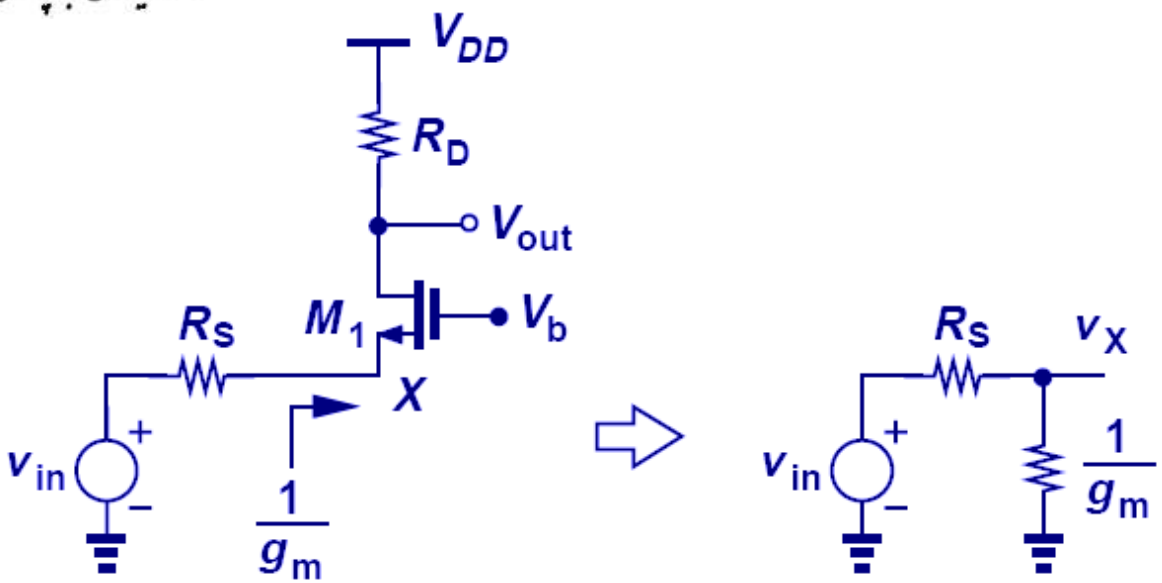
$$R_{in} = \frac{1}{g_m}$$

$$\lambda = 0$$

$$R_{out} = R_D$$

- **The input and output impedances of CG stage are similar to those of CB stage.**

CG Stage with Source Resistance



$$A_v = \frac{R_D}{\frac{1}{g_m} + R_S}$$

$$v_X = \frac{\frac{1}{g_m}}{\frac{1}{g_m} + R_S} v_{in}$$

$$= \frac{1}{1 + g_m R_S} v_{in}.$$

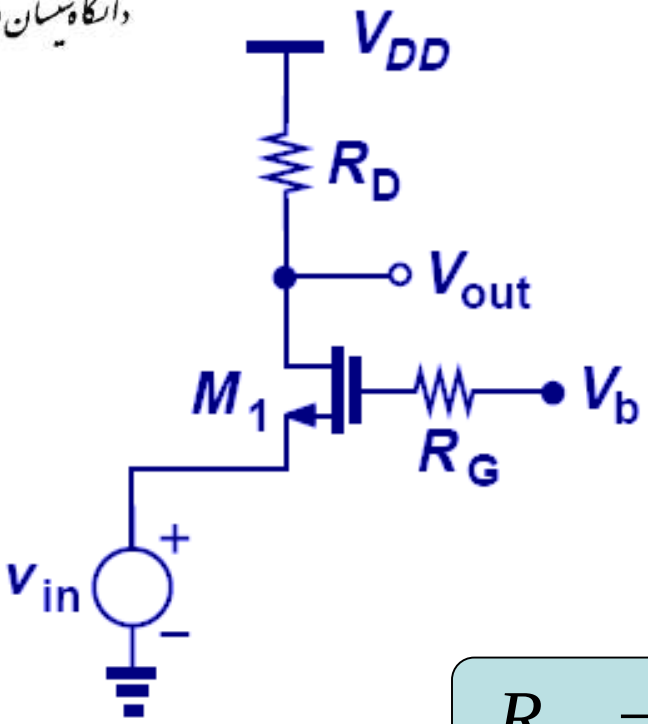
$$\frac{v_{out}}{v_{in}} = \frac{v_{out}}{v_X} \cdot \frac{v_X}{v_{in}}$$

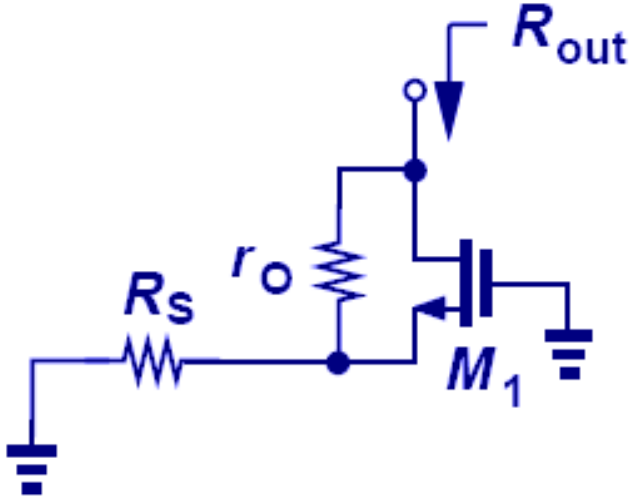
$$= \frac{g_m R_D}{1 + g_m R_S}$$

$$= \frac{R_D}{\frac{1}{g_m} + R_S}.$$

- **When a source resistance is present, the voltage gain is equal to that of a CS stage with degeneration, only positive.**

Generalized CG Behavior

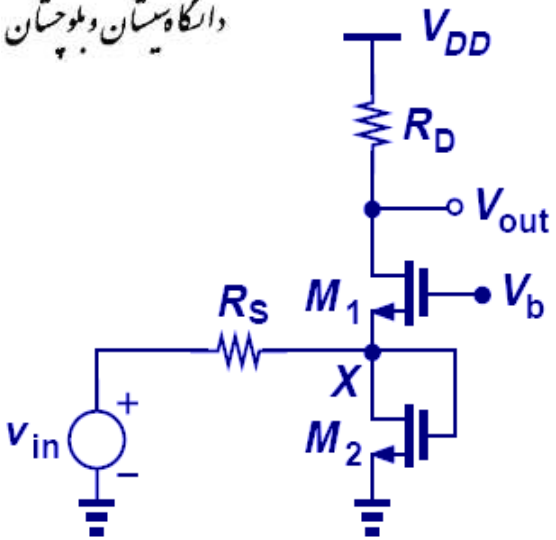


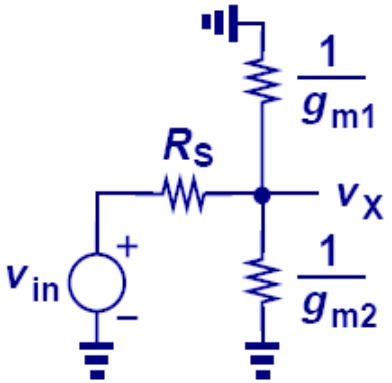


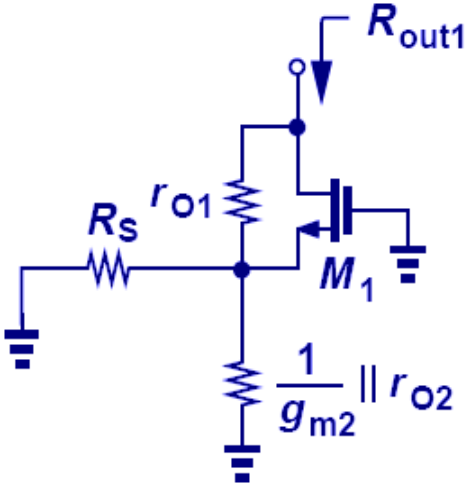
$$R_{out} = (1 + g_m r_O) R_S + r_O$$

- When a gate resistance is present it does not affect the gain and I/O impedances since there is no potential drop across it (at low frequencies).
- The output impedance of a CG stage with source resistance is identical to that of CS stage with degeneration.

Example 7.13: CG Stage





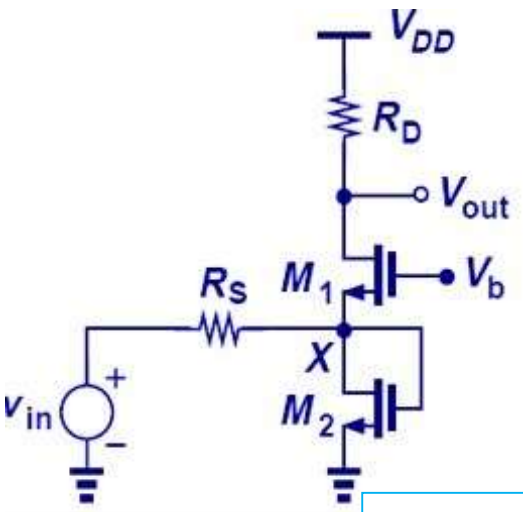


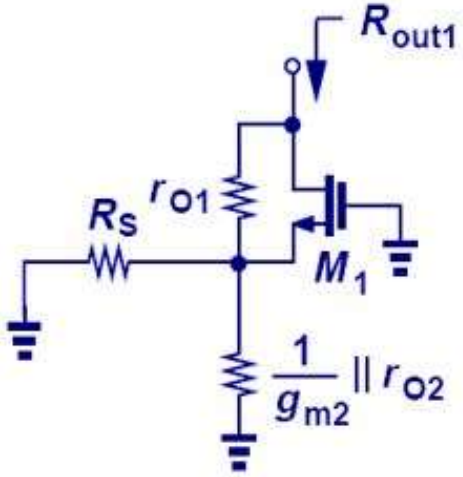
$$\frac{v_X}{v_{in}} = \frac{\frac{1}{g_{m2}} \| \frac{1}{g_{m1}}}{\frac{1}{g_{m2}} \| \frac{1}{g_{m1}} + R_S} = \frac{1}{1 + (g_{m1} + g_{m2})R_S}.$$

$$v_{out}/v_X = g_{m1}R_D,$$

$$\frac{v_{out}}{v_{in}} = \frac{g_{m1}R_D}{1 + (g_{m1} + g_{m2})R_S}.$$

Example 7.13: CG Stage





در فرمول کلی جایگذاری شود

$$= (1 + g_m r_O) R_S + r_O$$

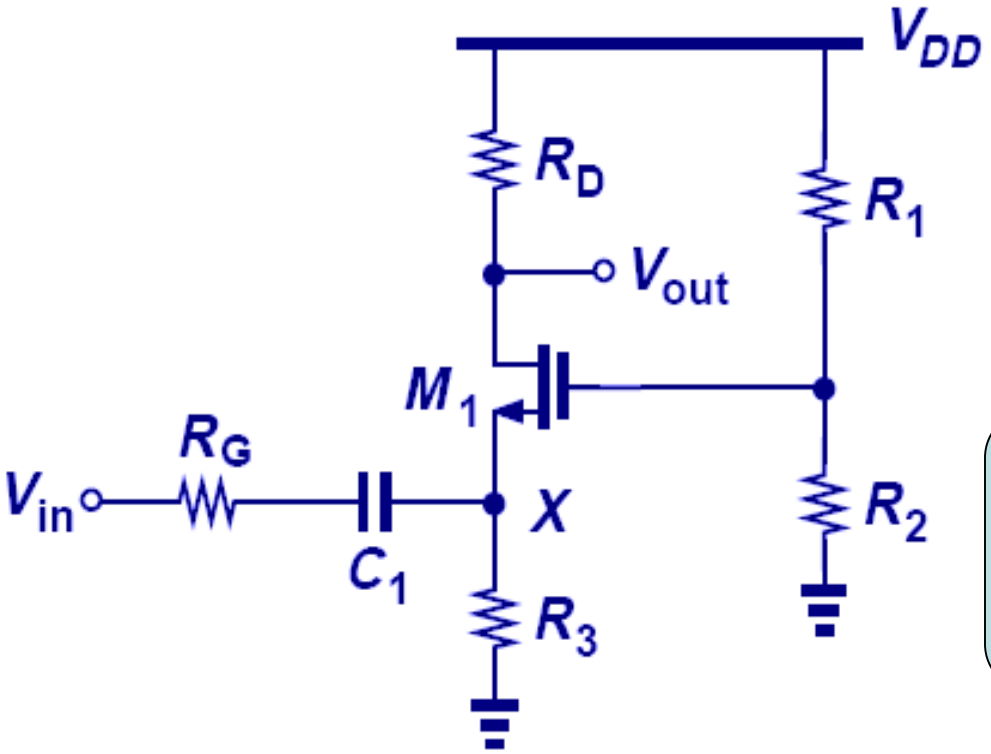
$$R_{out1} = (1 + g_{m1} r_{O1})(\frac{1}{g_{m2}} || r_{O2} || R_S) + r_{O1}$$

$$\approx g_{m1} r_{O1}(\frac{1}{g_{m2}} || R_S) + r_{O1}.$$

$$R_{out} = R_{out1} || R_D$$

$$\approx [g_{m1} r_{O1}(\frac{1}{g_{m2}} || R_S) + r_{O1}] || R_D.$$

CG Stage with Biasing



$$\frac{v_{out}}{v_{in}} = \frac{v_X}{v_{in}} \cdot \frac{v_{out}}{v_X}$$

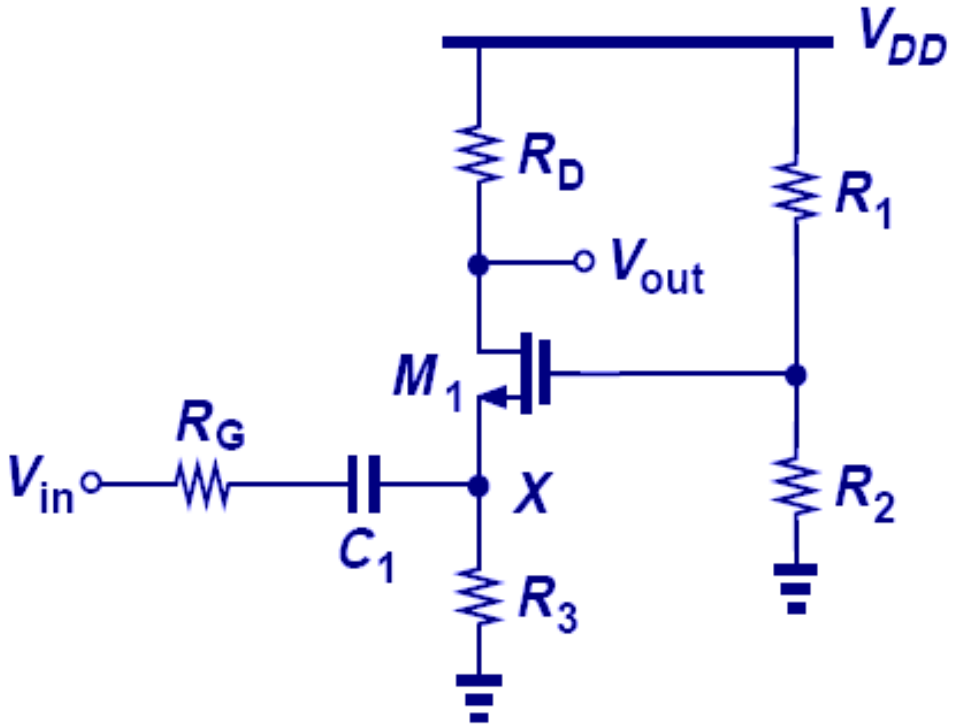
$$\frac{v_{out}}{v_{in}} = \frac{R_3 \| (1/g_m)}{R_3 \| (1/g_m) + R_S} \cdot g_m R_D$$

- R_1 and R_2 provide gate bias voltage, and R_3 provides a path for DC bias current of M_1 to flow to ground.

Example 7.14:

Example 7.14

Design the common-gate stage of Fig. 7.27 for the following parameters: $v_{out}/v_{in} = 5$, $R_S = 0$, $R_3 = 500\ \Omega$, $1/g_m = 50\ \Omega$, power budget $= 2$ mW, $V_{DD} = 1.8$ V. Assume $\mu_n C_{ox} = 100\ \mu\text{A/V}^2$, $V_{TH} = 0.5$ V, and $\lambda = 0$.



Example 7.14:

Solution

From the power budget, we obtain a total supply current of 1.11 mA. Allocating 10 μA to the voltage divider, R_1 and R_2, we leave 1.1 mA for the drain current of M_1. Thus, the voltage drop across R_3 is equal to 550 mV.

We must now compute two interrelated parameters: W/L and R_D. A larger value of W/L yields a greater g_m, allowing a lower value of R_D. As in Example 7.11, we choose an initial value for V_{GS} to arrive at a reasonable guess for W/L. For example, if $V_{GS} = 0.8$ V, then $W/L = 244$, and $g_m = 2I_D/(V_{GS} - V_{TH}) = (136.4\ \Omega)^{-1}$, dictating $R_D = 682\ \Omega$ for $v_{out}/v_{in} = 5$.

Let us determine whether M_1 operates in saturation. The gate voltage is equal to V_{GS} plus the drop across R_3, amounting to 1.35 V. On the other hand, the drain voltage is given by $V_{DD} - I_D R_D = 1.05$ V. Since the drain voltage exceeds $V_G - V_{TH}$, M_1 is indeed in saturation.

The resistive divider consisting of R_1 and R_2 must establish a gate voltage equal to 1.35 V while drawing 10 μA:

$$\frac{V_{DD}}{R_1 + R_2} = 10\ \mu\text{A} \tag{7.120}$$

$$\frac{R_2}{R_1 + R_2} V_{DD} = 1.35\ \text{V}. \tag{7.121}$$

It follows that $R_1 = 45\ \text{k}\Omega$ and $R_2 = 135\ \text{k}\Omega$.

Example 7.15:

Example 7.15

Suppose in Example 7.14, we wish to minimize W/L (and hence transistor capacitances). What is the minimum acceptable value of W/L?

Solution

For a given I_D, as W/L decreases, $V_{GS} - V_{TH}$ increases. Thus, we must first compute the maximum allowable V_{GS}. We impose the condition for saturation as

$$V_{DD} - I_D R_D > V_{GS} + V_{R3} - V_{TH}, \tag{7.122}$$

$$\frac{2I_D}{V_{GS} - V_{TH}} R_D = A_v.$$

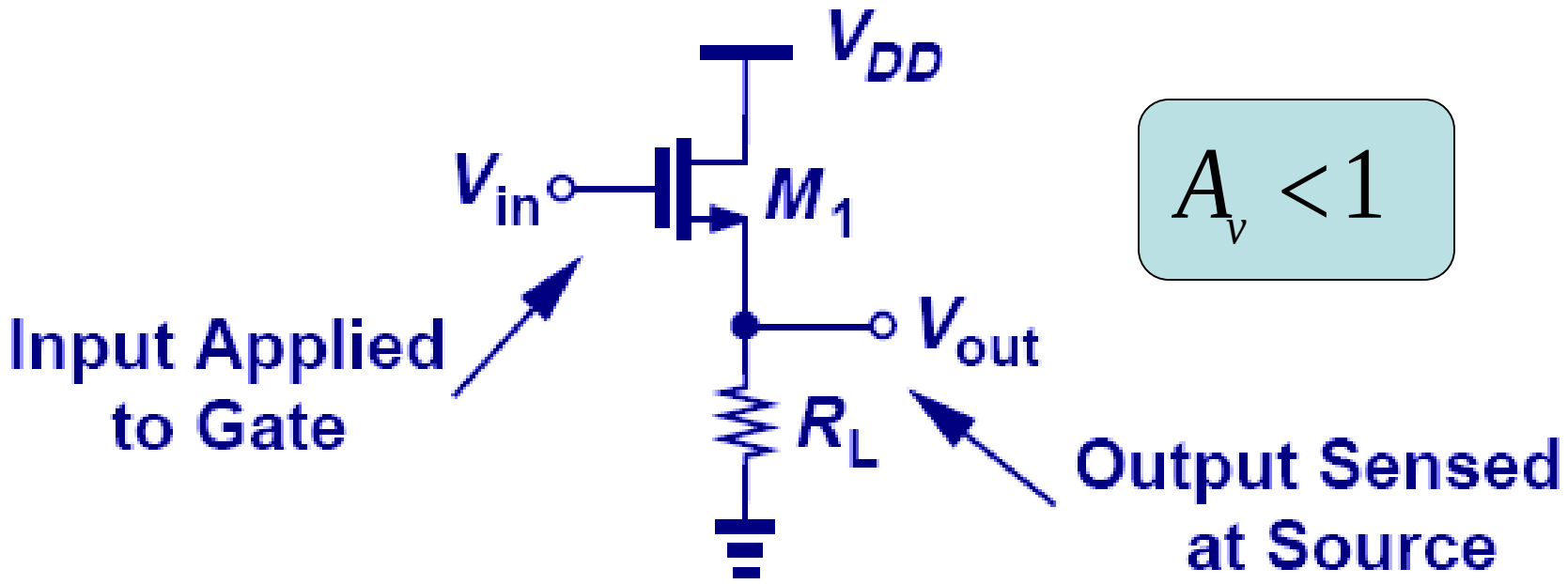
$$V_{DD} - \frac{A_v}{2}(V_{GS} - V_{TH}) > V_{GS} - V_{TH} + V_{R3}$$

$$V_{GS} - V_{TH} < \frac{V_{DD} - V_{R3}}{\frac{A_v}{2} + 1}.$$

$$W/L > \frac{2I_D}{\mu_n C_{ox} \left(2\frac{V_{DD} - V_{R3}}{A_v + 2}\right)^2}.$$

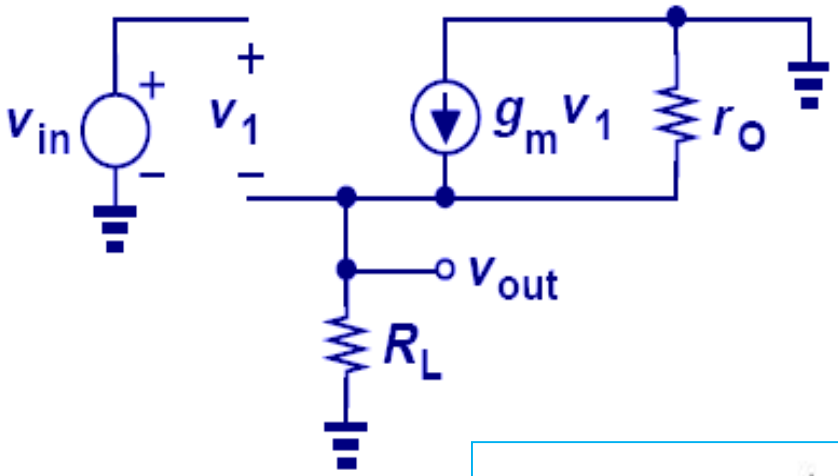
$$W/L > 172.5.$$

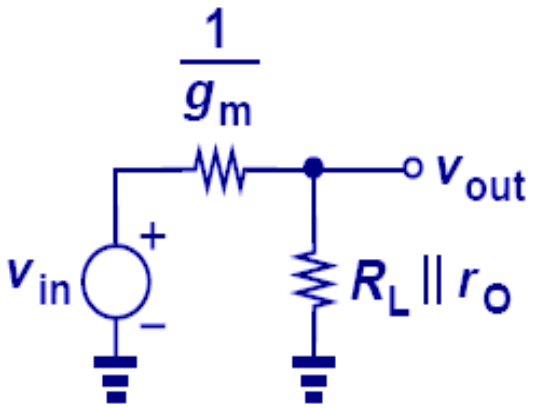
Source Follower Stage



$$A_v < 1$$

Source Follower Core





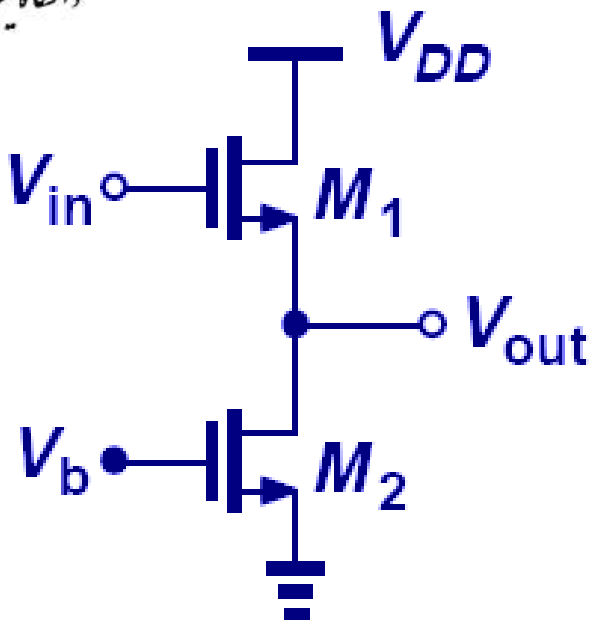
$$v_{in} = v_1 + v_{out}.$$

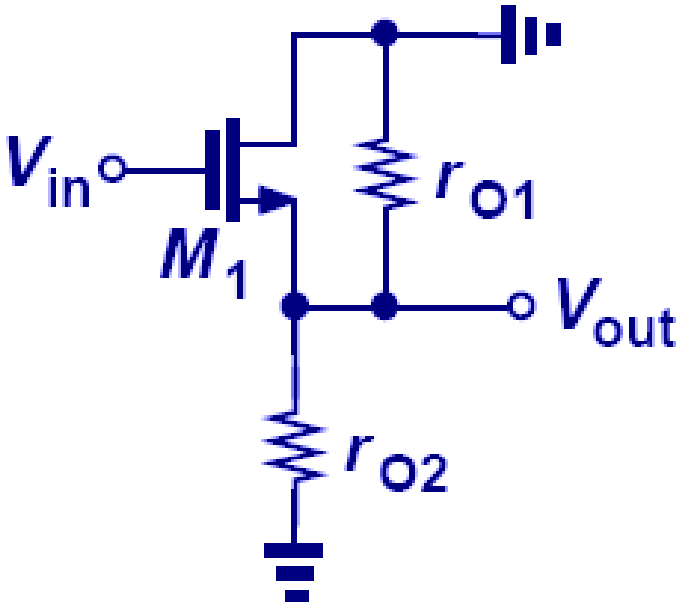
$$\frac{v_{out}}{v_{in}} = \frac{g_m(r_O||R_L)}{1+g_m(r_O||R_L)}$$

$$= \frac{r_O||R_L}{\frac{1}{g_m}+r_O||R_L}.$$

$$\frac{v_{out}}{v_{in}} = \frac{r_O \| R_L}{\frac{1}{g_m}+r_O \| R_L}$$

Example 7.16: Source Follower

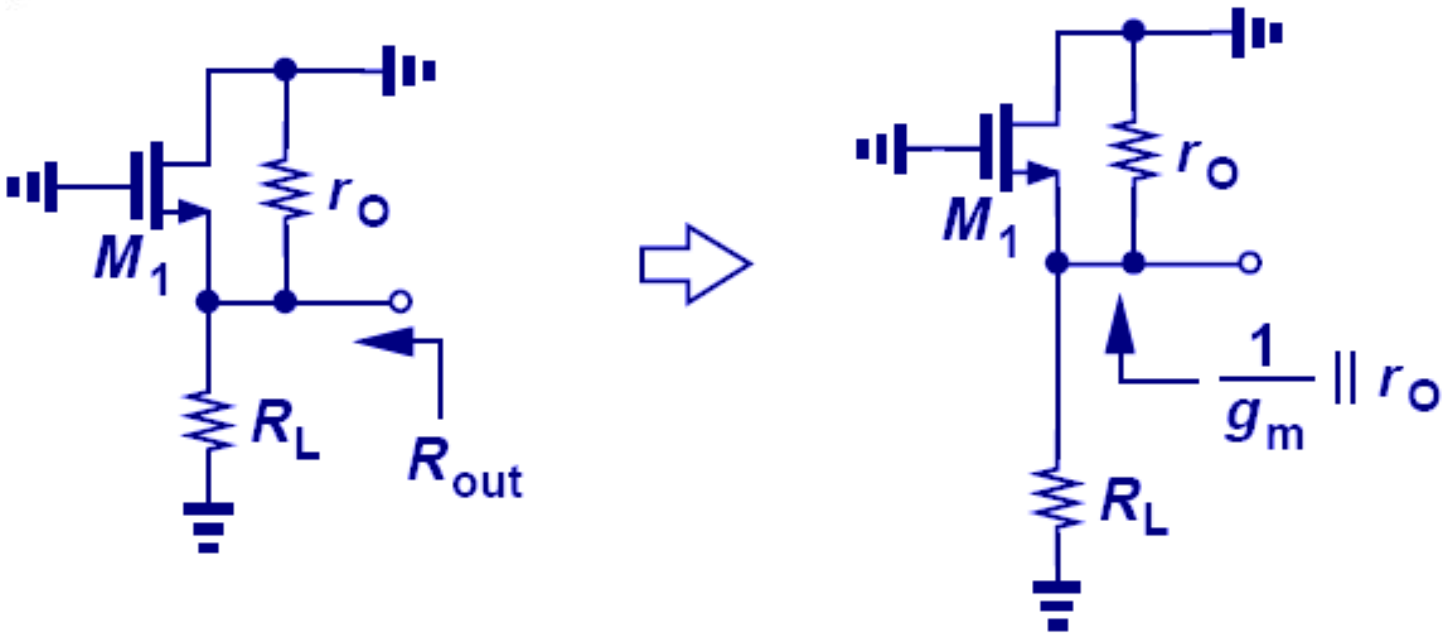




$$A_v = \frac{r_{O1} \parallel r_{O2}}{\dfrac{1}{g_{m1}} + r_{O1} \parallel r_{O2}}$$

- In this example, M_2 acts as a current source.

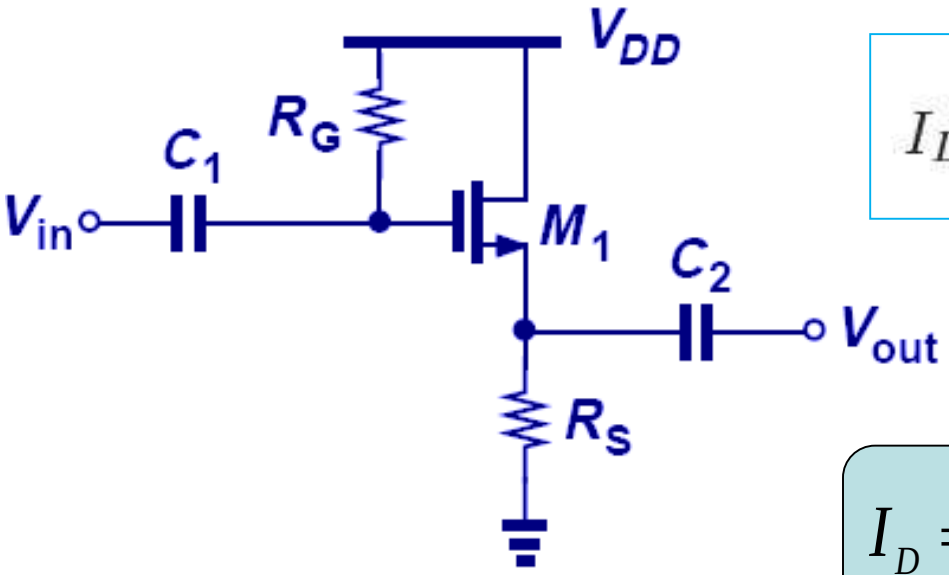
Output Resistance of Source Follower



$$R_{out} = \frac{1}{g_m} \| r_O \| R_L \approx \frac{1}{g_m} \| R_L$$

- **The output impedance of a source follower is relatively low, whereas the input impedance is infinite (at low frequencies); thus, a good candidate as a buffer.**

Source Follower with Biasing



$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2$$

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{DD} - I_D R_S - V_{TH})^2$$

- R_G sets the gate voltage to V_{DD}, whereas R_S sets the drain current.
- The quadratic equation above can be solved for I_D.

Example 7.18: Source Follower with Biasing

Example 7.18

Design the source follower of Fig. 7.32 for a drain current of 1 mA and a voltage gain of 0.8. Assume $\mu_n C_{ox} = 100\ \mu\text{A/V}^2$, $V_{TH} = 0.5$ V, $\lambda = 0$, $V_{DD} = 1.8$ V, and $R_G = 50\ \text{k}\Omega$.

Solution

The unknowns in this problem are V_{GS}, W/L, and R_S. The following three equations can be formed:

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2 \tag{7.141}$$

$$I_D R_S + V_{GS} = V_{DD} \tag{7.142}$$

$$A_v = \frac{R_S}{\dfrac{1}{g_m} + R_S}.$$

If g_m is written as $2I_D/(V_{GS} - V_{TH})$,

Solution

Example 7.18: Source Follower with Biasing

If g_m is written as $2I_D/(V_{GS}-V_{TH})$,

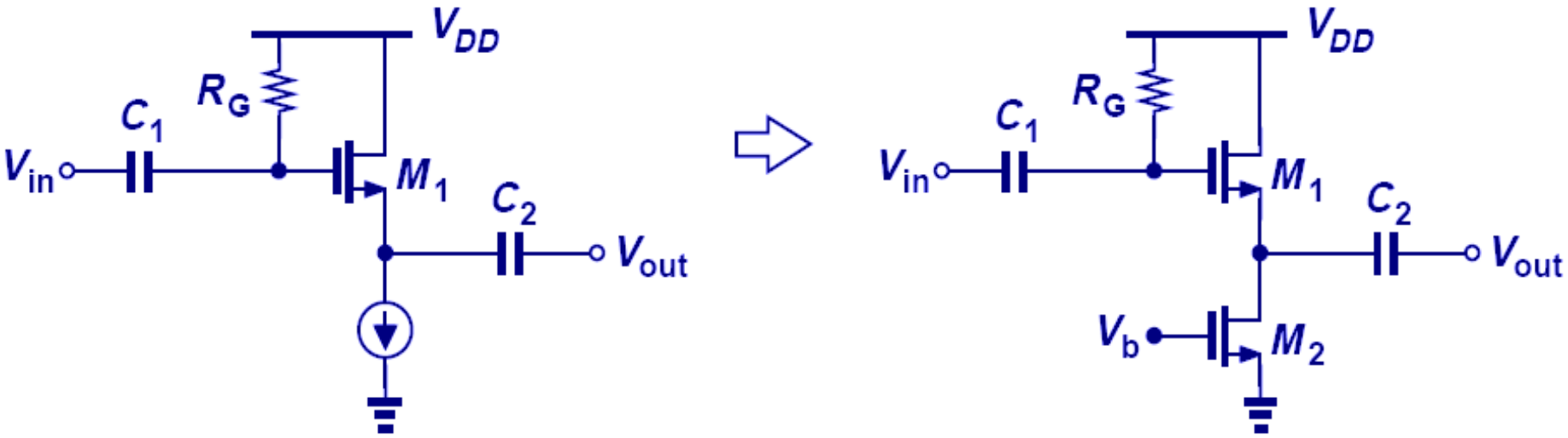
$$A_v = \frac{R_S}{\frac{V_{GS}-V_{TH}}{2I_D}+R_S}$$
$$= \frac{2I_D R_S}{V_{GS}-V_{TH}+2I_D R_S}$$
$$= \frac{2I_D R_S}{V_{DD}-V_{TH}+I_D R_S}.$$

$$R_S = \frac{V_{DD}-V_{TH}}{I_D}\frac{A_v}{2-A_v}$$
$$= 867\,\Omega.$$

$$V_{GS} = V_{DD} - I_D R_S$$
$$= V_{DD} - (V_{DD}-V_{TH})\frac{A_v}{2-A_v}$$
$$= 0.933\ \text{V}.$$

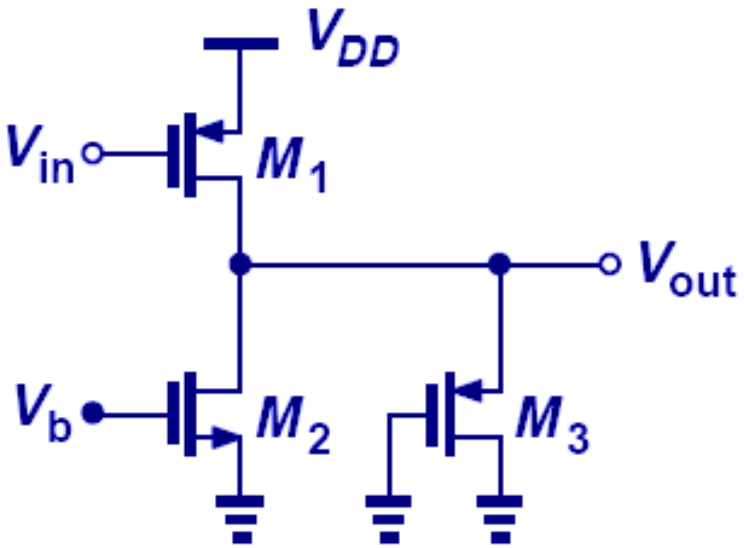
$$\frac{W}{L} = 107.$$

Supply-Independent Biasing

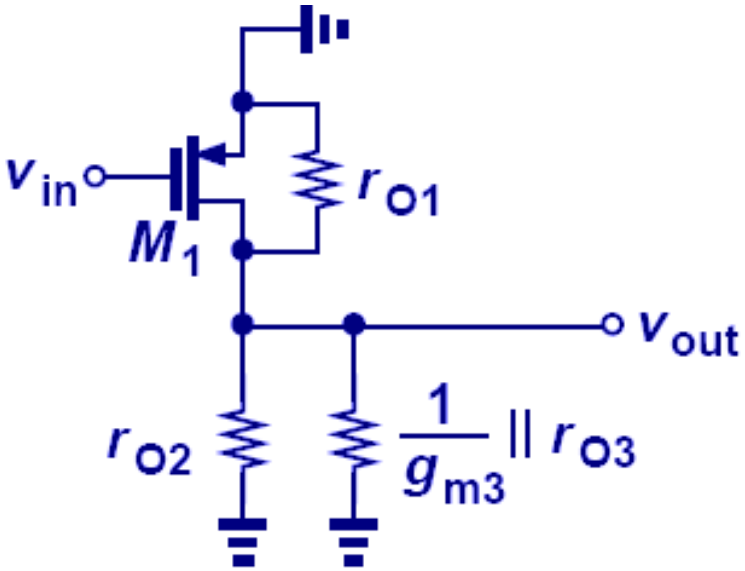


- If R_s is replaced by a current source, drain current I_D becomes independent of supply voltage.

Example of a CS Stage (I) (7.19)



(a)



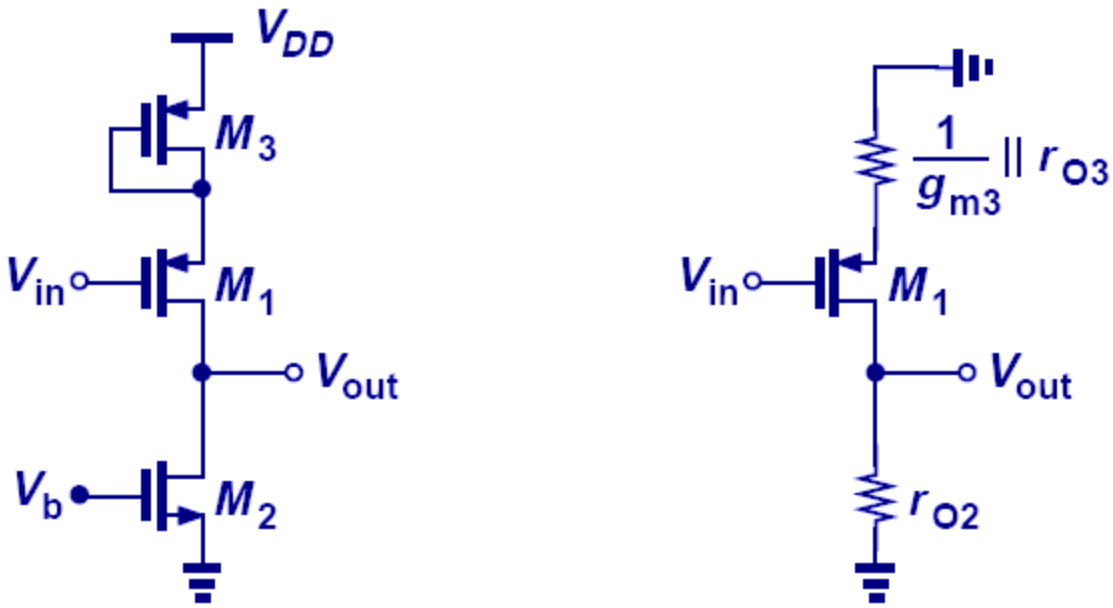
(b)

$$A_v = -g_{m1}\left(\frac{1}{g_{m3}} \| r_{O1} \| r_{O2} \| r_{O3}\right)$$

$$R_{out} = \frac{1}{g_{m3}} \| r_{O1} \| r_{O2} \| r_{O3}$$

- M_1 acts as the input device and M_2, M_3 as the load.

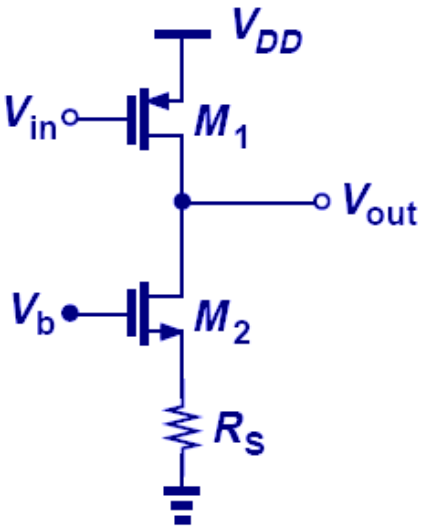
Example of a CS Stage (II) (7.20)



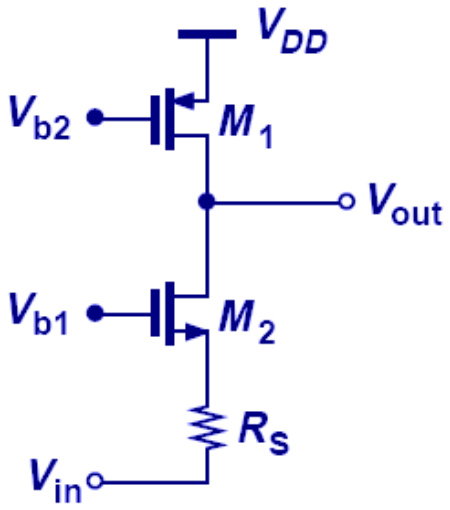
$$A_v = -\frac{r_{O2}}{\frac{1}{g_{m1}} + \frac{1}{g_{m3}} \| r_{O3}}$$

- **M_1 acts as the input device, M_3 as the source resistance, and M_2 as the load.**

Examples of CS and CG Stages (7.21)



(a)



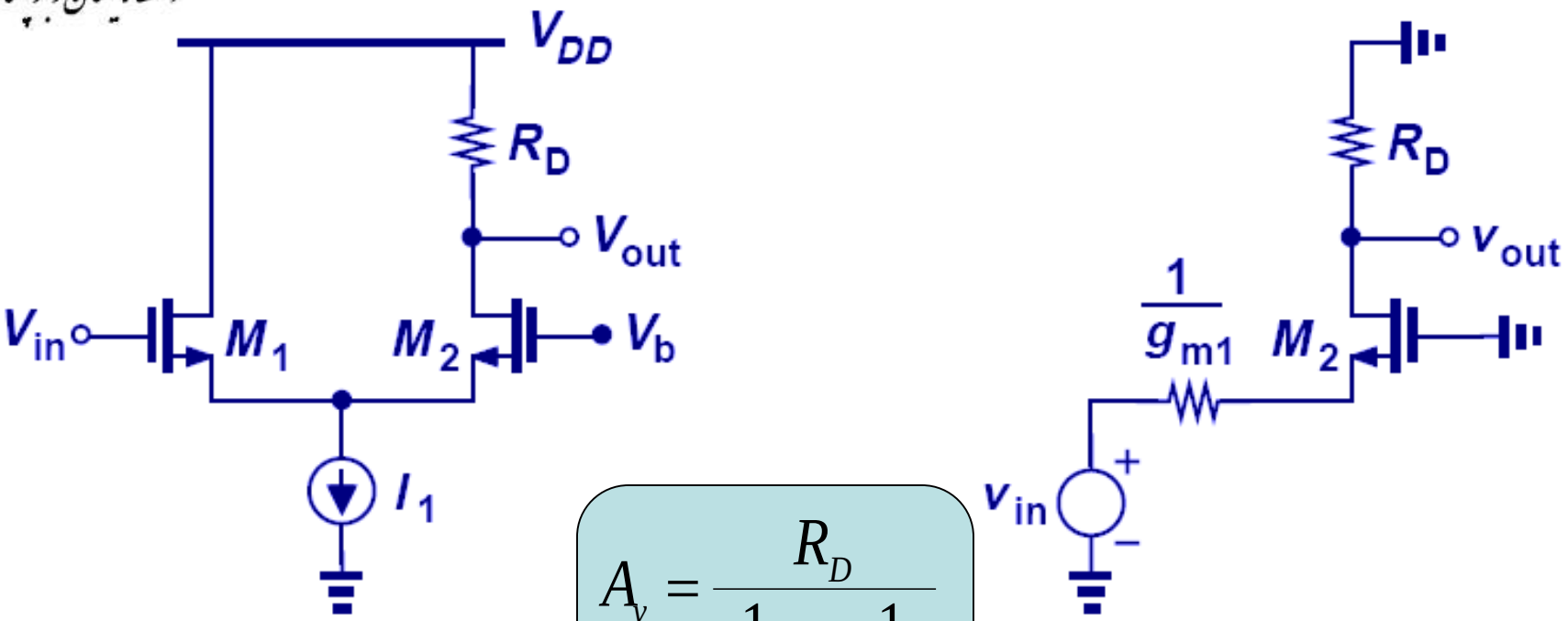
(b)

$$A_{v\_CS} = -g_{m2}\left[(1+g_{m1}r_{O1})R_S + r_{O1}\right] \| \, r_{O1}$$

$$A_{v\_CG} = \frac{r_{O2}}{\frac{1}{g_m} + R_S}$$

- **With the input connected to different locations, the two circuits, although identical in other aspects, behave differently.**

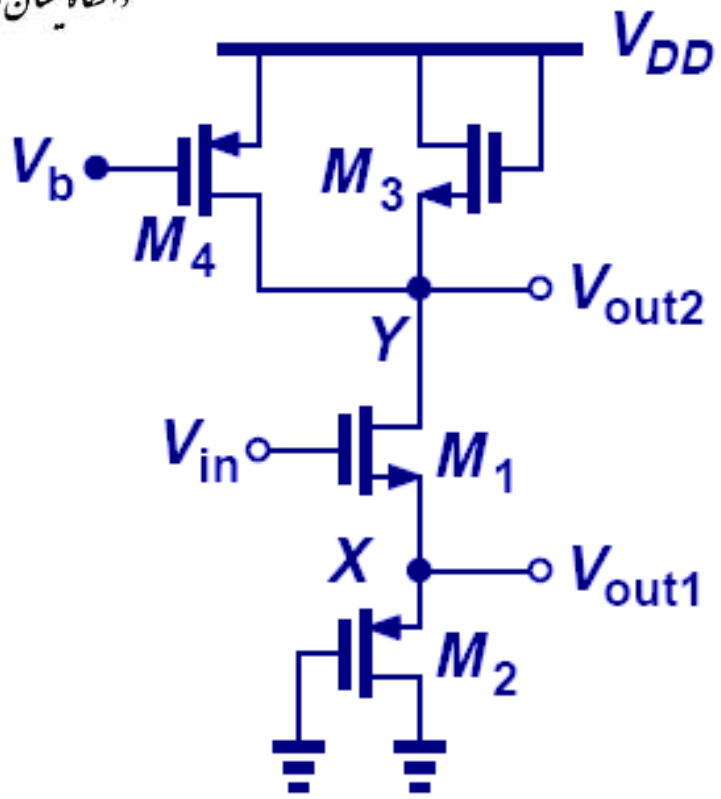
Example of a Composite Stage (I) (7.22)



$$A_v = \frac{R_D}{\frac{1}{g_{m1}} + \frac{1}{g_{m2}}}$$

- **By replacing the left side with a Thevenin equivalent, and recognizing the right side is actually a CG stage, the voltage gain can be easily obtained.**

Example of a Composite Stage (II) (7.23)



$$\frac{v_{out1}}{v_{in}} = \frac{\frac{1}{g_{m2}} || r_{O2}}{\frac{1}{g_{m2}} || r_{O2} + \frac{1}{g_{m1}}}.$$

$$\frac{v_{out2}}{v_{in}} = -\frac{\frac{1}{g_{m3}} \| r_{O3} \| r_{O4}}{\frac{1}{g_{m2}} \| r_{O2} + \frac{1}{g_{m1}}}$$

خدایا شکر