Fundamentals of Microelectronics II

مثال فصل ۱۵– مدارهای دیجیتال CMOS

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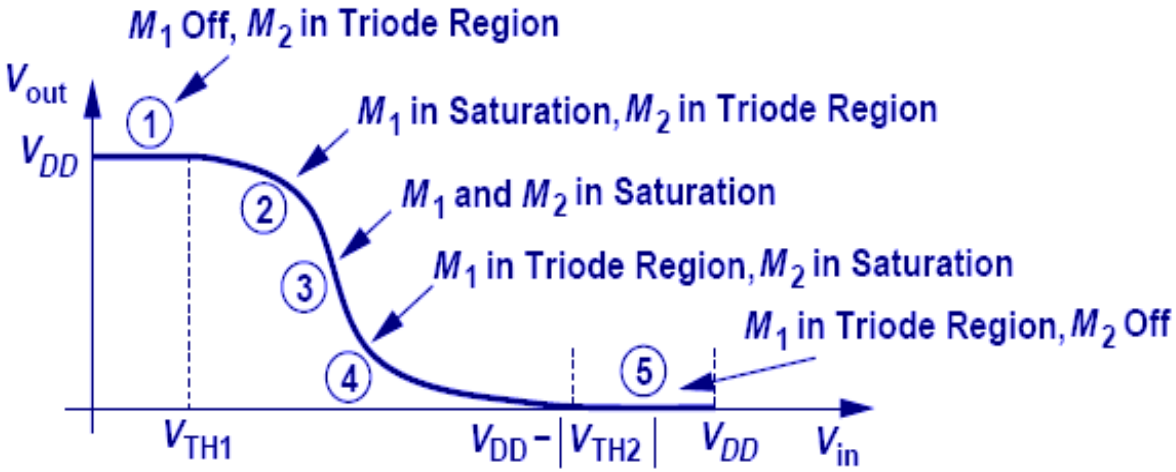
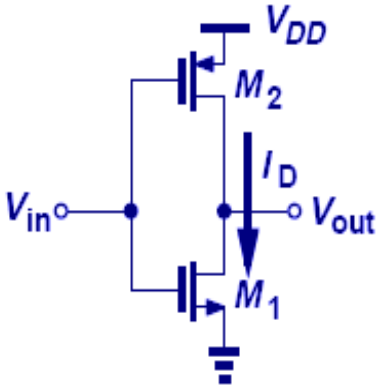
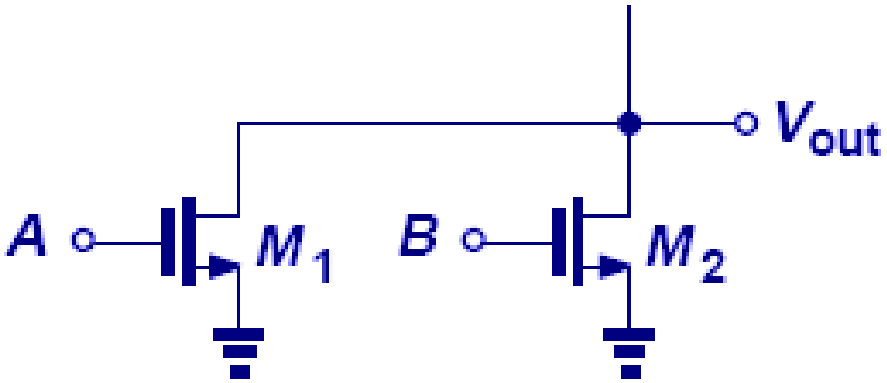
CMOS Inverter VTC



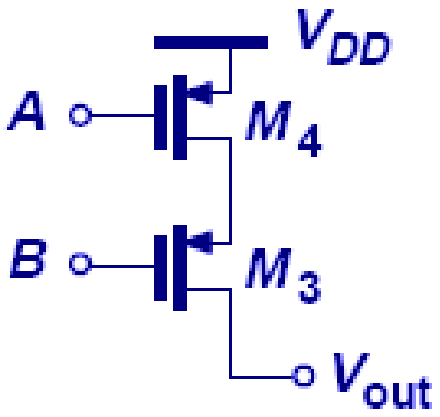


NMOS Section of NOR



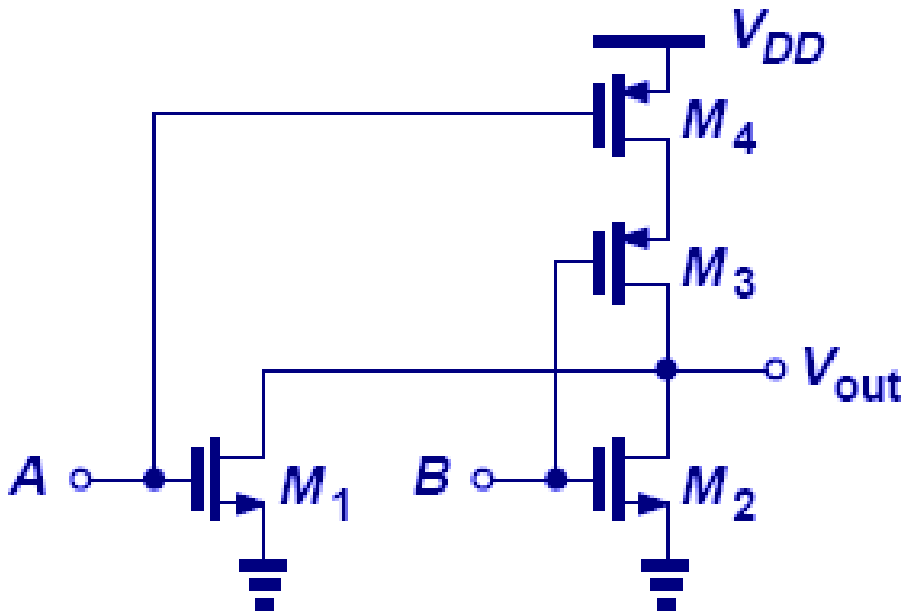
- **When either A or B is high or if both A and B are high, the output will be low. Transistors operate as pull-down devices.**

PMOS Section of NOR



- **When both A and B are low, the output is high. Transistors operate as pull-up devices.**

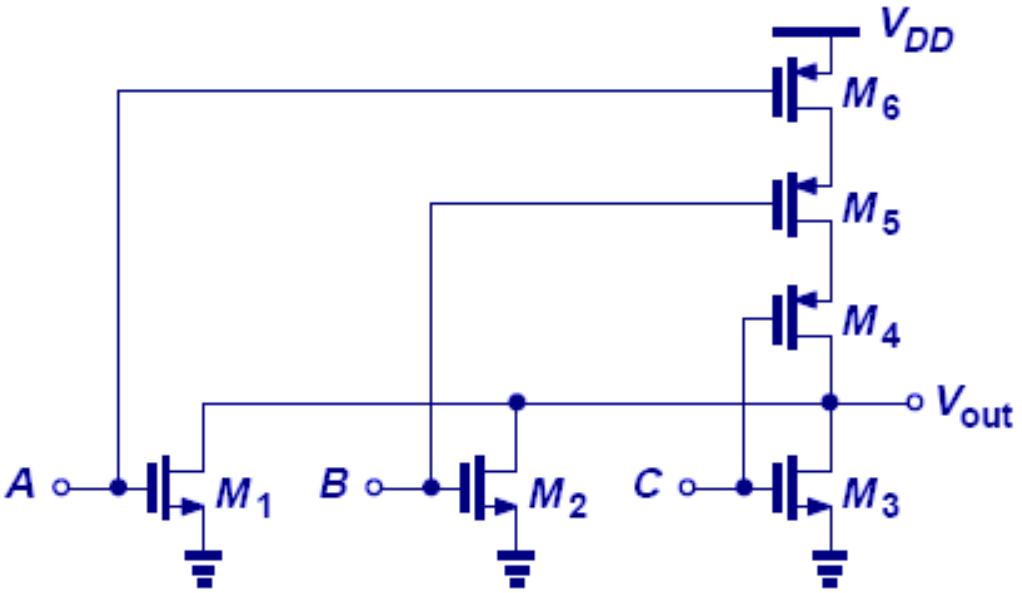
CMOS NOR



$$Vout=\overline{(A+B)}$$

- **Combing the NMOS and PMOS NOR sections, we have the CMOS NOR.**

Example: Three-Input NOR



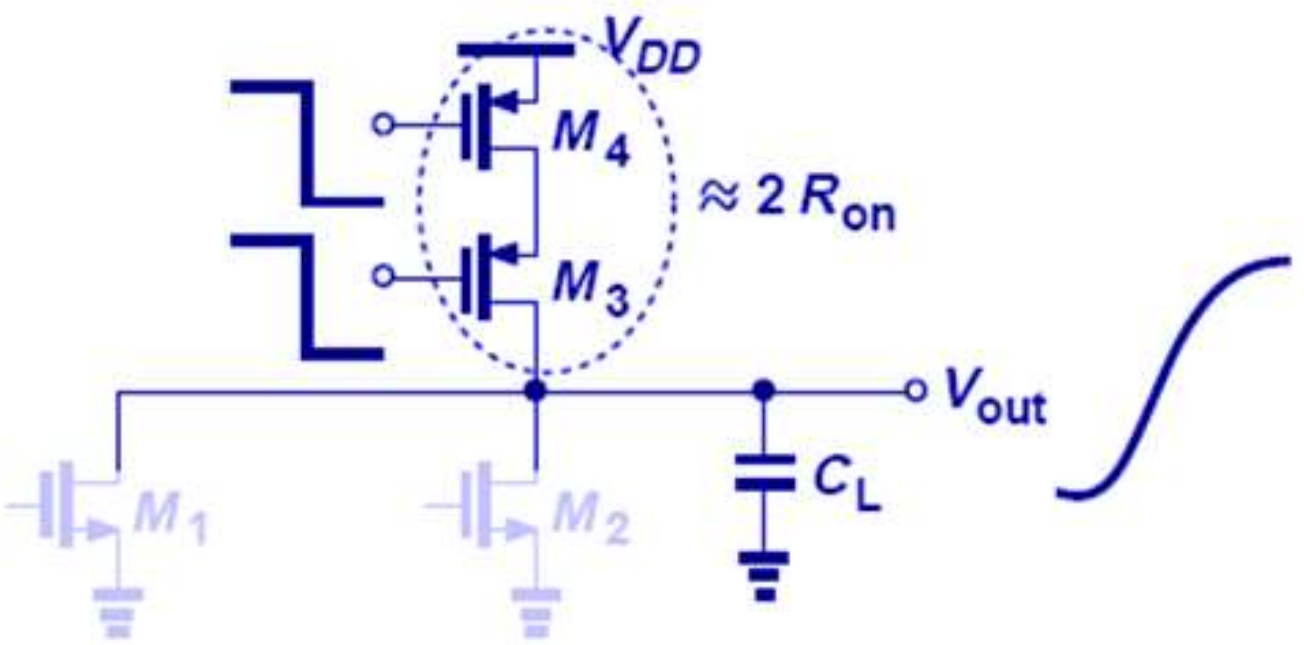
$$V_{out} = \left(A + B + C\right)'$$

Equal Rise & Fall ($\mu_n \approx 2\mu_p$)

$W_1=W_2=W_3=W$

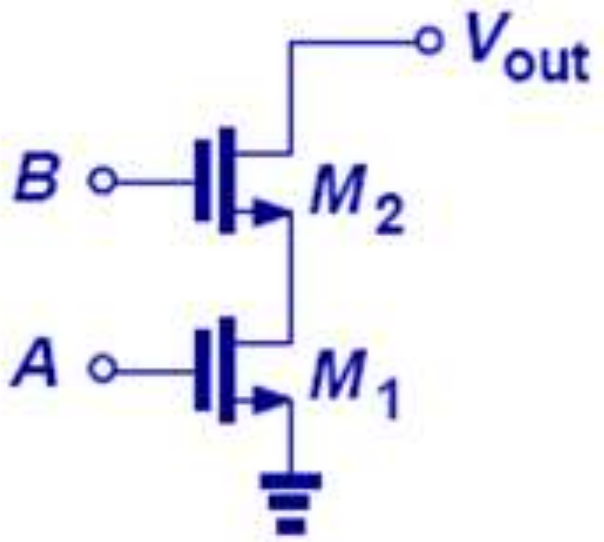
$W_4=W_5=W_6=6W$

Drawback of CMOS NOR



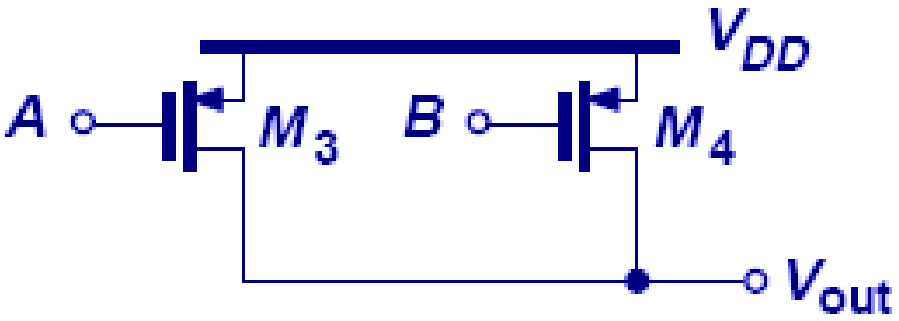
- **Due to low PMOS mobility, series combination of M_3 and M_4 suffers from a high resistance, producing a long delay.**
- **The widths of the PMOS transistors can be increased to counter the high resistance, however this would load the preceding stage and the overall delay of the system may not improve.**

NMOS NAND Section



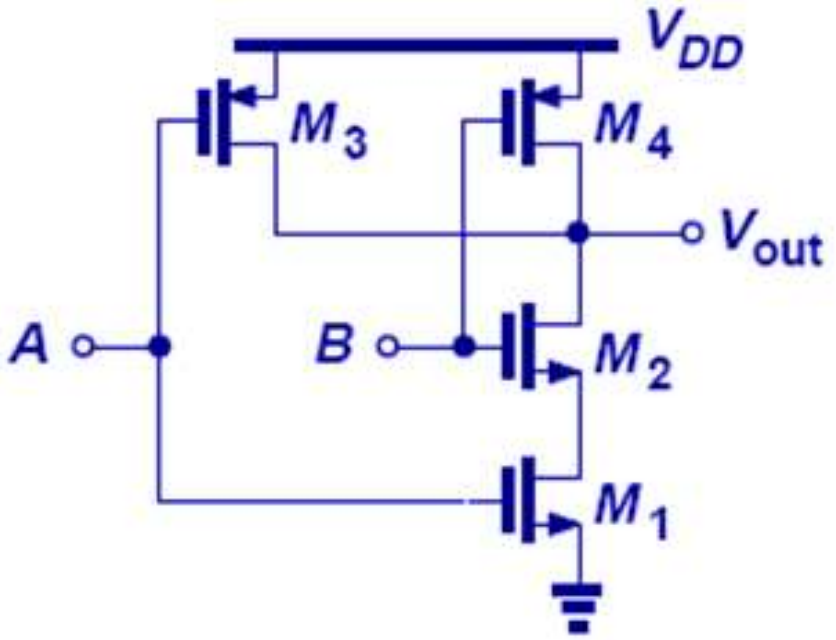
- **When both A and B are high, the output is low.**

PMOS NOR Section



- **When either A or B is low or if both A and B are low, the output is high.**

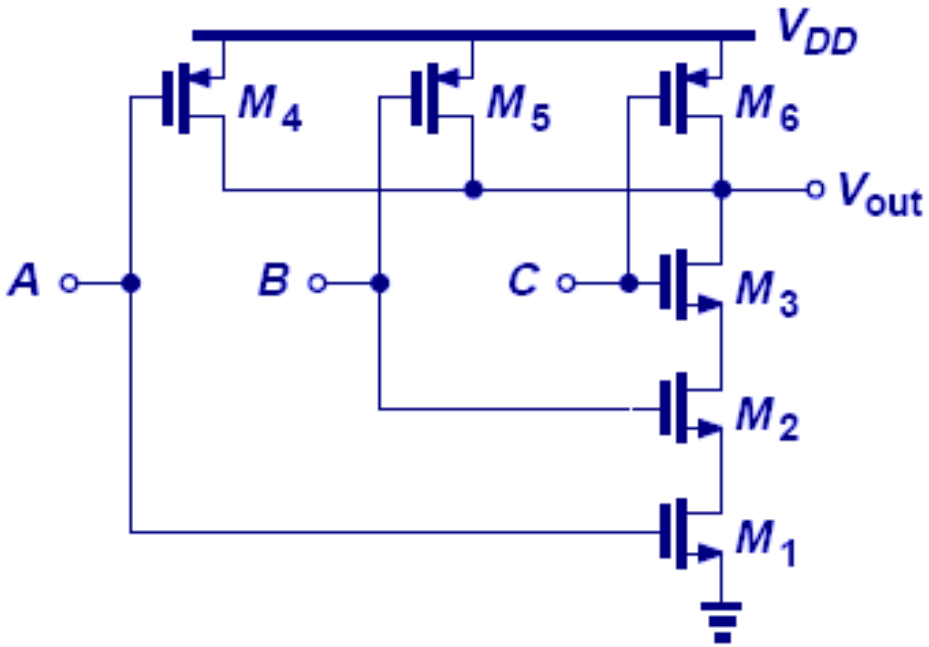
CMOS NAND



$$Vout=\overline{(A.B)}$$

- **Just like the CMOS NOR, the CMOS NAND can be implemented by combining its respective NMOS and PMOS sections, however it has better performance because its PMOS transistors are not in series.**

Example: Three-Input NAND



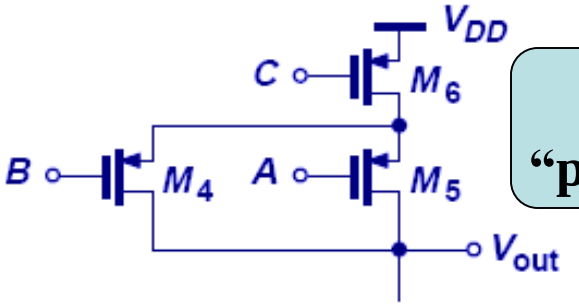
$$V_{out} = (ABC)'$$

Equal Rise & Fall ($\mu_n \approx 2\mu_p$)

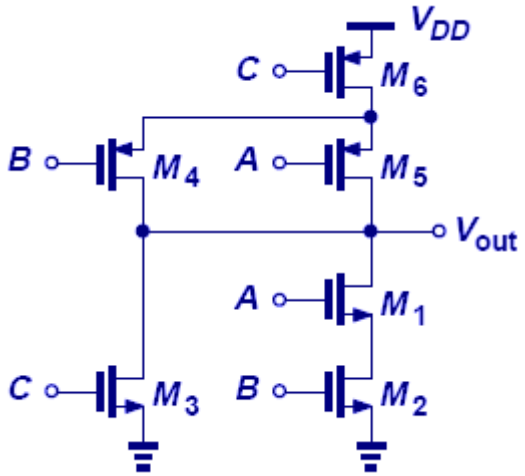
$W_1=W_2=W_3=3W$

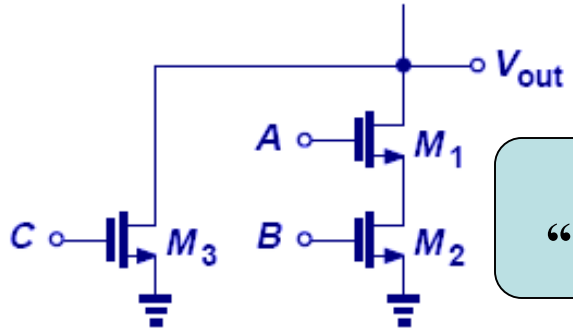
$W_4=W_5=W_6=2W$

NMOS and PMOS Duality



C is in "series" with the "parallel" combination of A and B





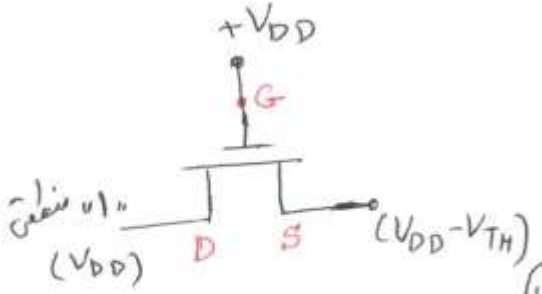
C is in "parallel" with the "series" combination of A and B

- **In the CMOS philosophy, the PMOS section can be obtained from the NMOS section by converting series combinations to the parallel combinations and vice versa.**

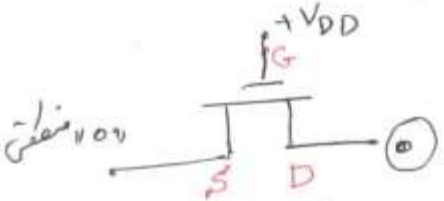
سوییچ MOS

سوییچ MOS:

- یک ضعیف: NMOS
- صفر خوب: "



("1" منطقی، با اندازه V_{TH} تضعیف یافته است)



انتقال صفر (خوب)

توجه: ① عموماً ترانزیستور باید در ناحیه Triode باشد تا بتوانیم بعنوان سوییچ استفاده کنیم.

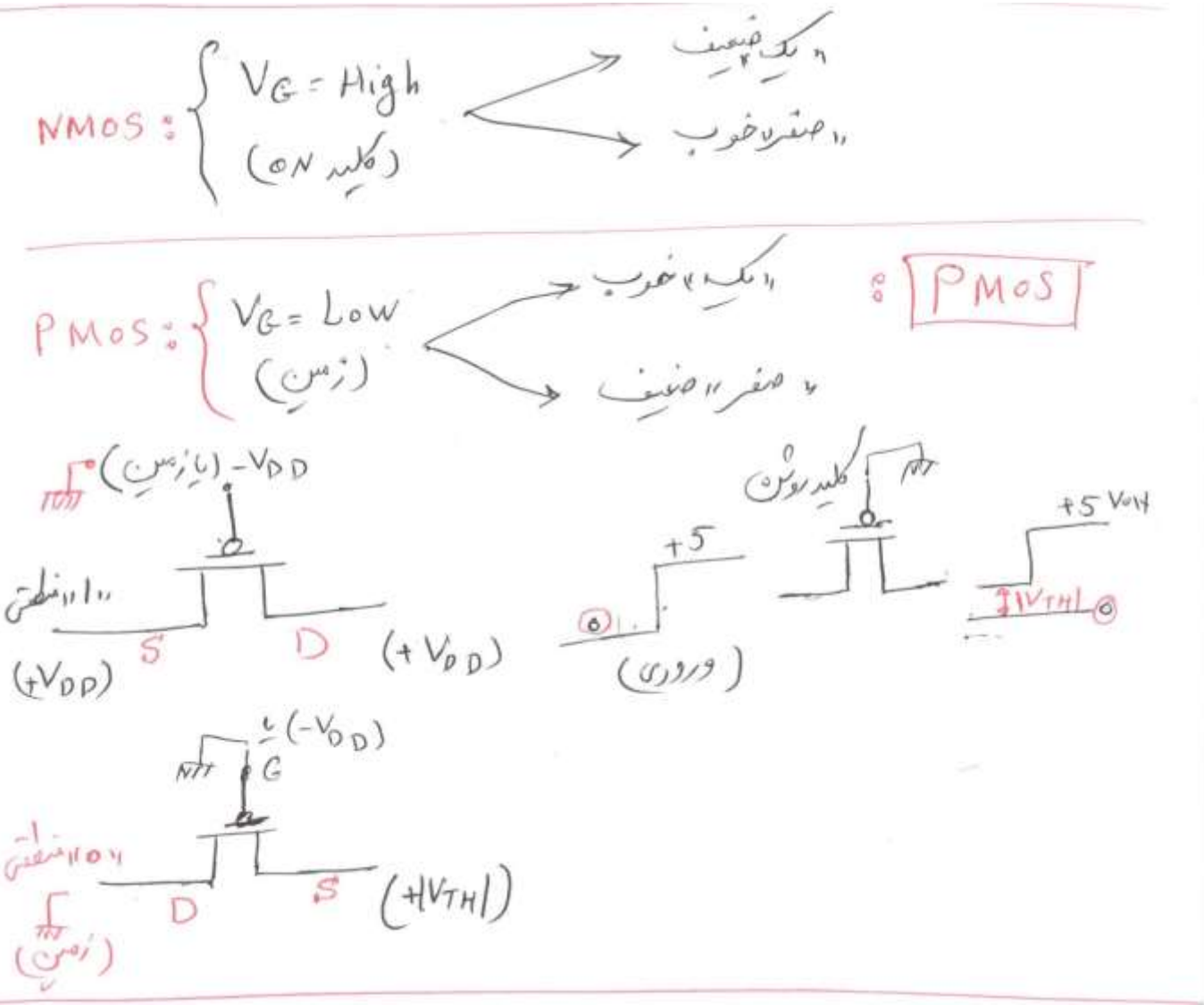
V_G = High ($+V_{DD}$) ⟶ کلید روشن (ON) ⟶

② شرط Triode:

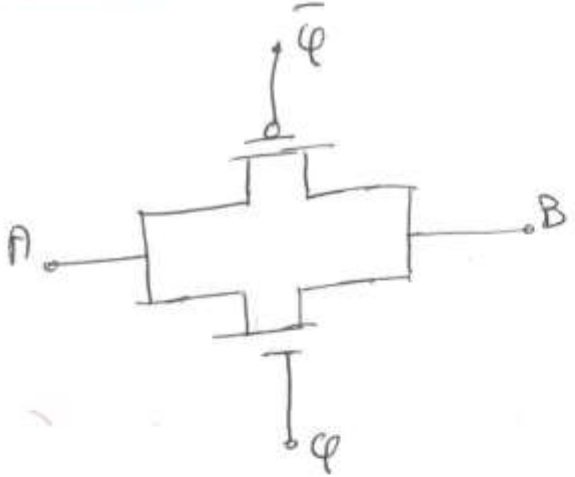
۱- باید $|V_{GS}| > V_{TH}$ (برای روشن)

۲- باید $|V_{DS}| < (V_{GS}-V_{TH})$ باشد (یعنی $V_{DS} \to 0$)

سوییچ MOS


NMOS :
VG = High
(ON کلید)
یک ضعیف
صفر خوب
PMOS :
VG = Low
(زمین)
یک خوب
صفر ضعیف
PMOS
-VDD
(یا زمین)
(+VDD)
S
D
(+VDD)
کلید روشن
+5
(ورودی)
+5 Volt
|VTH|
G
(-VDD)
D
S
(+|VTH|)
(زمین)

CMOS :



$\varphi = 0, \bar{\varphi} = 1 \Rightarrow$ حالت قطع کلید $\Rightarrow$ مدار باز

$\varphi = 1, \bar{\varphi} = 0 \Rightarrow$ حالت وصل کلید

$\Downarrow$

اتصال کوتاه

$\Leftarrow$ (هر دو ترانزیستور وصل هستند)

نتیجه دو مقاومت موازی $\Leftarrow$ یک مقاومت هم مقدار کمتر

در هنگام وصل کلید (که هر دو ترانزیستور در حالت Triode قرار دارند)

"1" منطقی از طریق PMOS منتقل می‌شود

"0" منطقی از طریق NMOS منتقل می‌شود

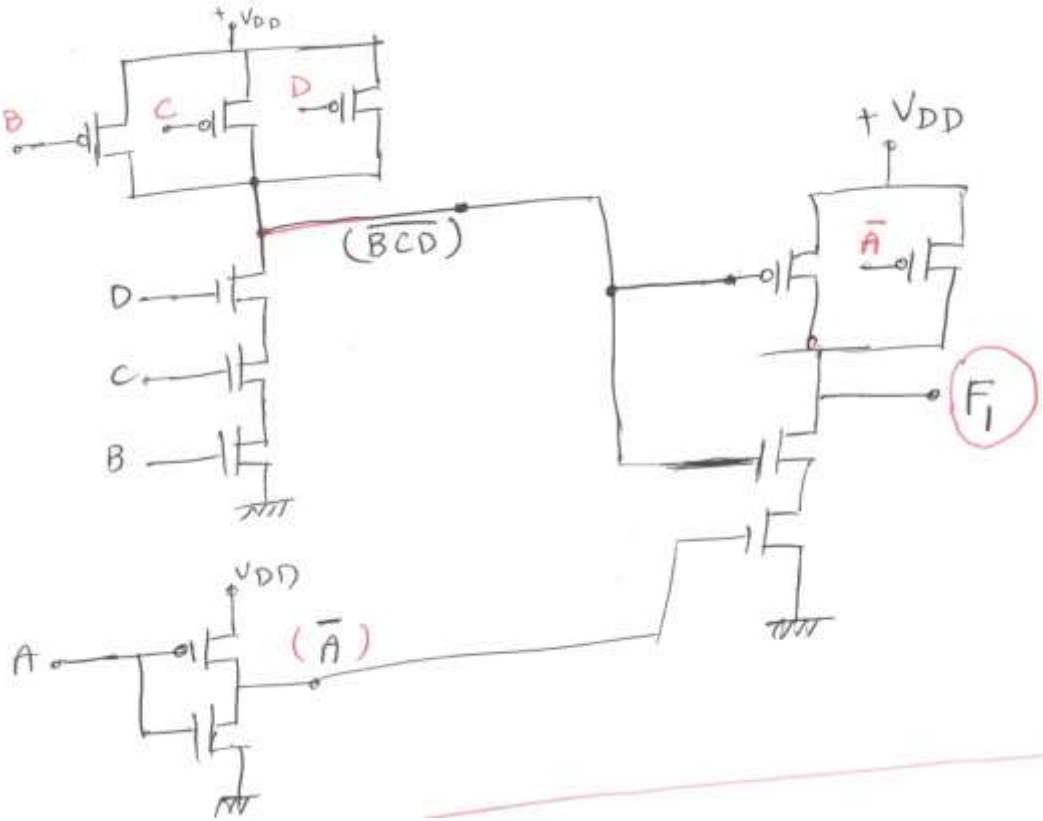
در نتیجه یک انتقال خوب هم برای "1" و هم برای "0" وجود دارد.

$\overline{A+B} = \bar{A} \cdot \bar{B}$, $\overline{A \cdot B} = \bar{A} + \bar{B}$

مثال ۱:

$F_1 = A + BCD$

$F_1 = \overline{A + BCD} = \bar{A} \cdot (\overline{BCD})$

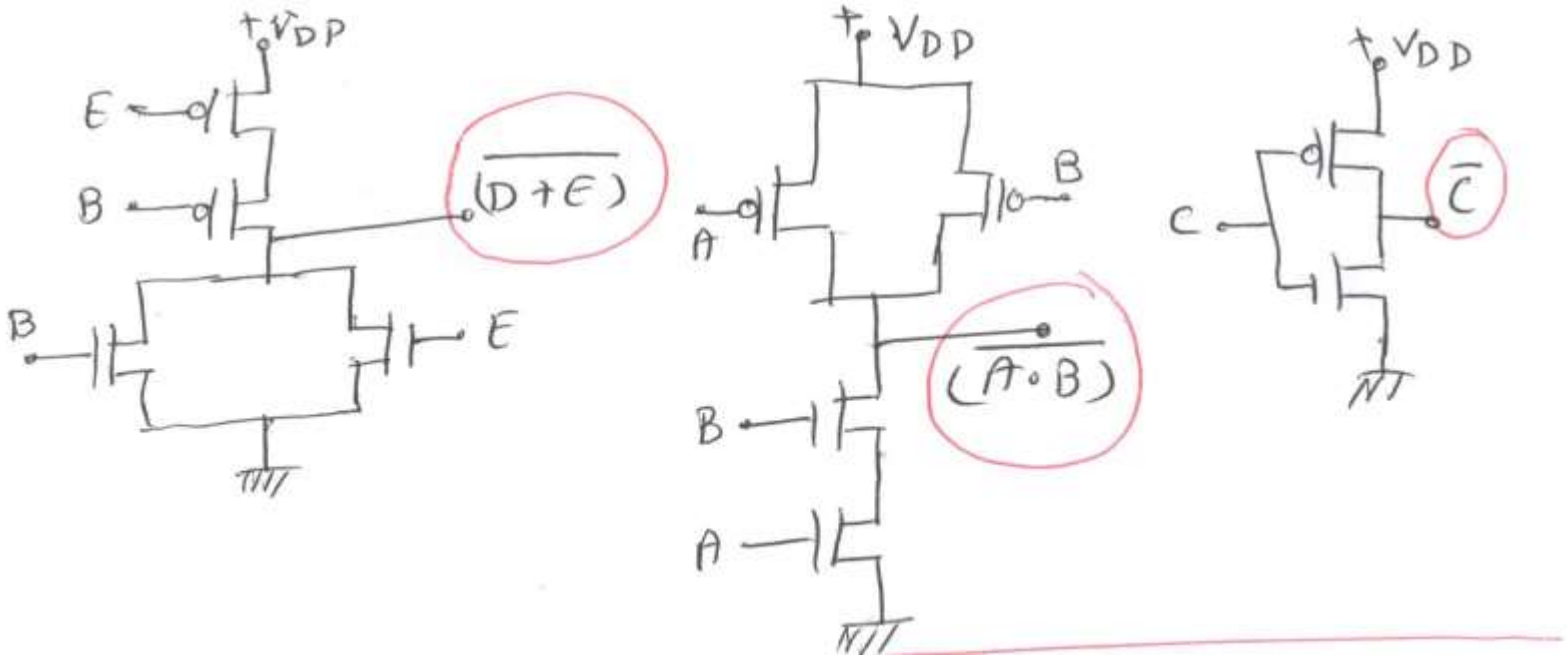


مثال ۲

مثال ۲:

$$f_2 = AB + C(D+E)$$

$$f_2 = \overline{\overline{AB + C\cdot(D+E)}} = \overline{\overline{AB}\cdot(\bar{C} + \overline{(D+E)})}$$



مثال ۲ (ادامه)