Fundamentals of Microelectronics II

فصل ۱۵– مدارهای دیجیتال CMOS

Mohammad Ali Mansouri- Birjandi
Majid Ghadrdan

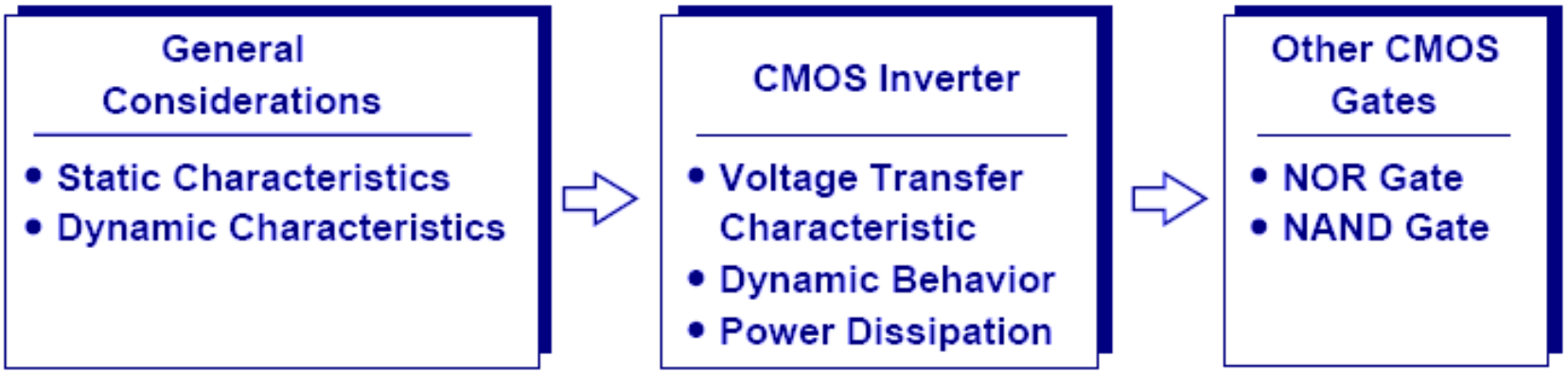
Faculty of Electrical and Computer Engineering
University of Sistan and Baluchestan (USB)

mansouri@ece.usb.ac.ir ,
mamansouri@yahoo.com

Chapter 15 Digital CMOS Circuits

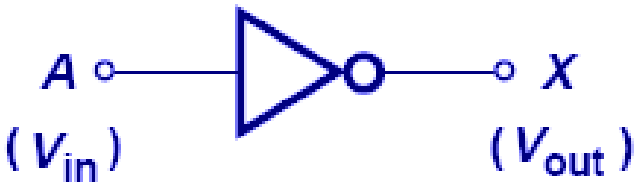
- 15.1 General Considerations
- 15.2 CMOS Inverter
- 15.3 CMOS NOR and NAND Gates

Chapter Outline

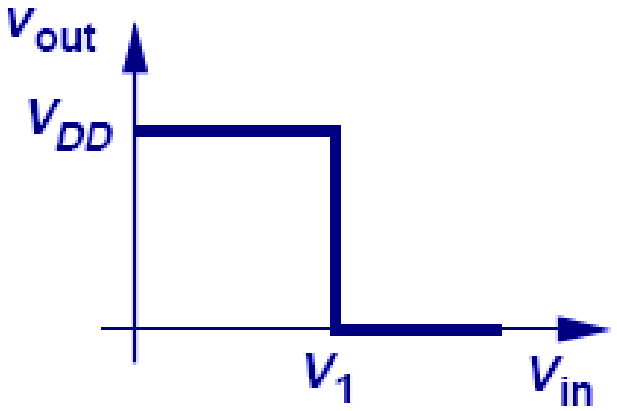


RDL ⇒ TTL ⇒ ECL ⇒ CMOS

Inverter Characteristic



(a)

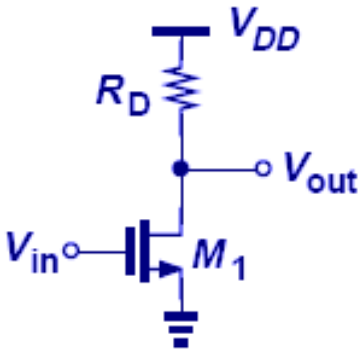


(b)

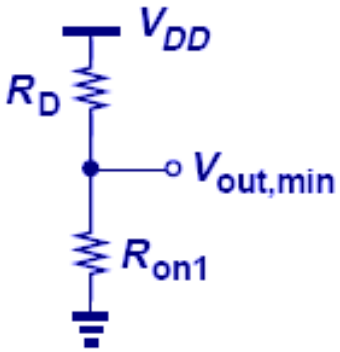
$$X = \bar{A}$$

- **An inverter outputs a logical “1” when the input is a logical “0” and vice versa.**

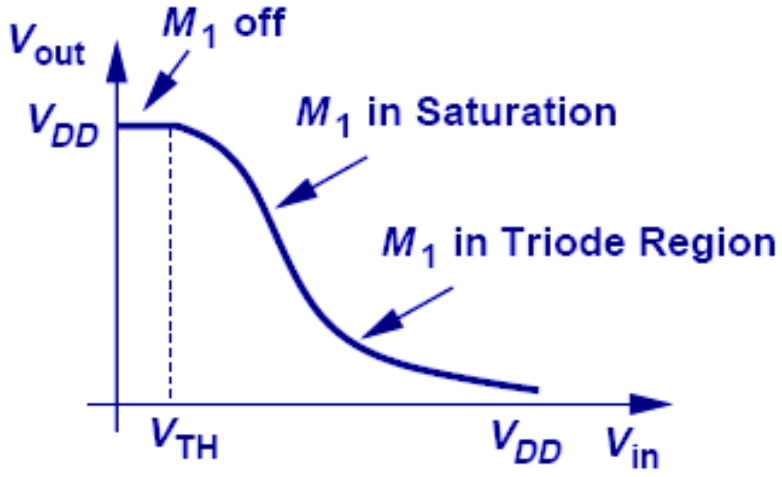
NMOS Inverter



(a)



(b)



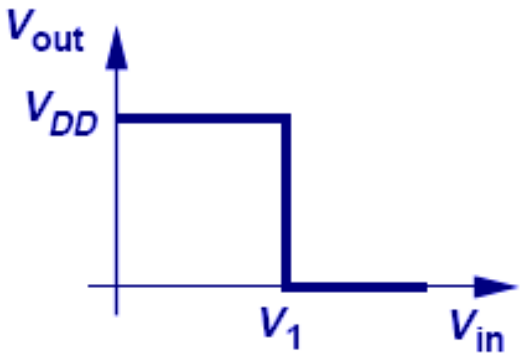
(c)

برای عملکرد سوییچ، (هنگام روشن شدن)
ترانزیستور حتما باید در ناحیه تریود قرار گیرد.

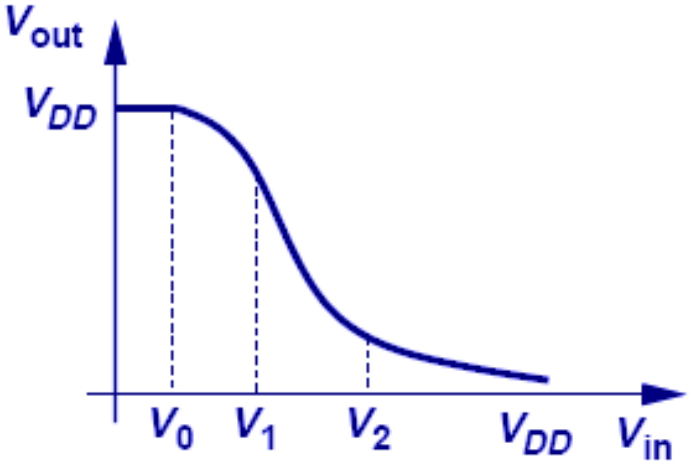
$$R_{on1} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{DD} - V_{TH})}$$

- The CS stage resembles a voltage divider between R_D and R_{on1} when M_1 is in deep triode region. It produces V_{DD} when M_1 is off.

Transition Region Gain



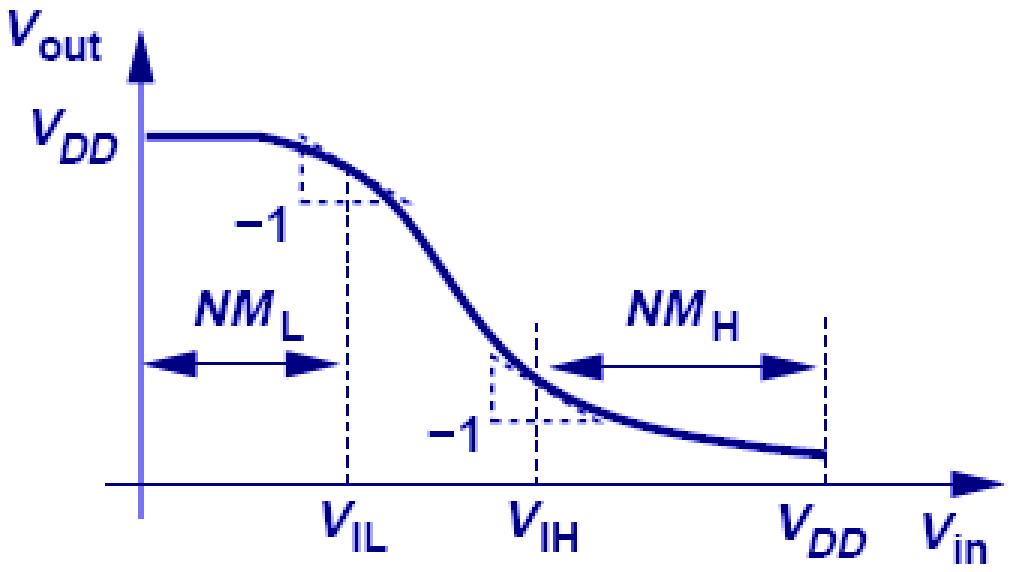
Infinite Transition Region Gain



Finite Transition Region Gain

- **Ideally, the VTC of an inverter has infinite transition region gain. However, practically the gain is finite.**

Noise Margin

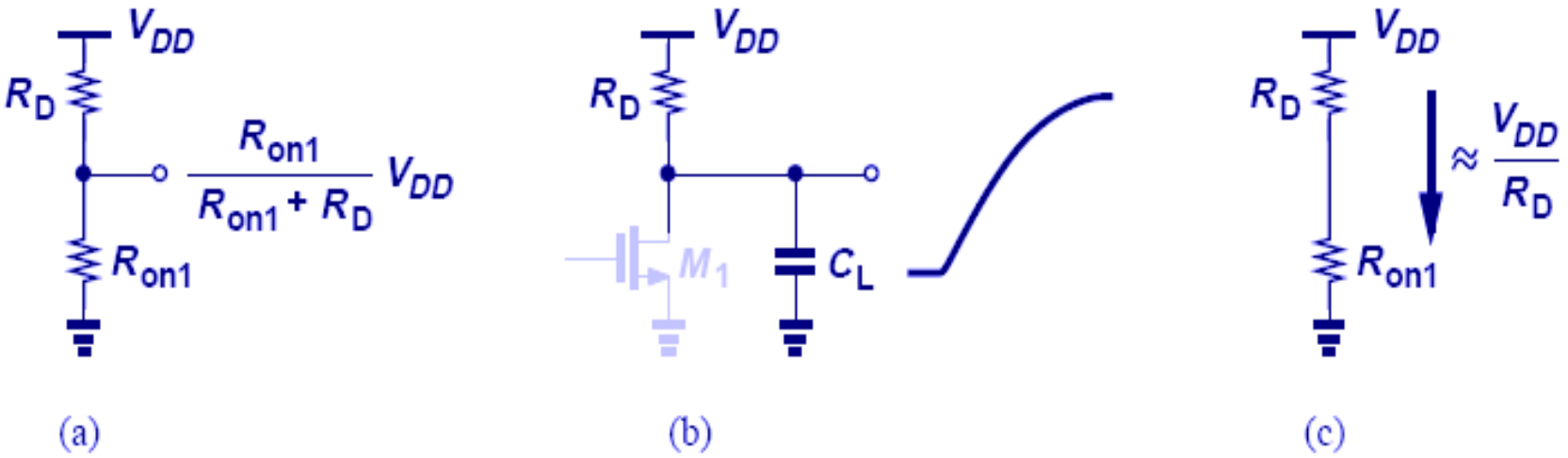


برای بیان کمی مقاومت گیت در برابرتغییر سطوح منطقی، از مفهوم حاشیه نویز استفاده می کنیم.

حاشیه نویز: ماکزیمم تغییر سطح ورودی (نویز) قابل تحمل است که به ازای آن خروجی تغییر شدیدی نمی کند.
یا : فاصله سطح ورودی ایده آل تا ورودی ای است که به ازای آن بهره سیگنال کوچک گیت، یک می شود.

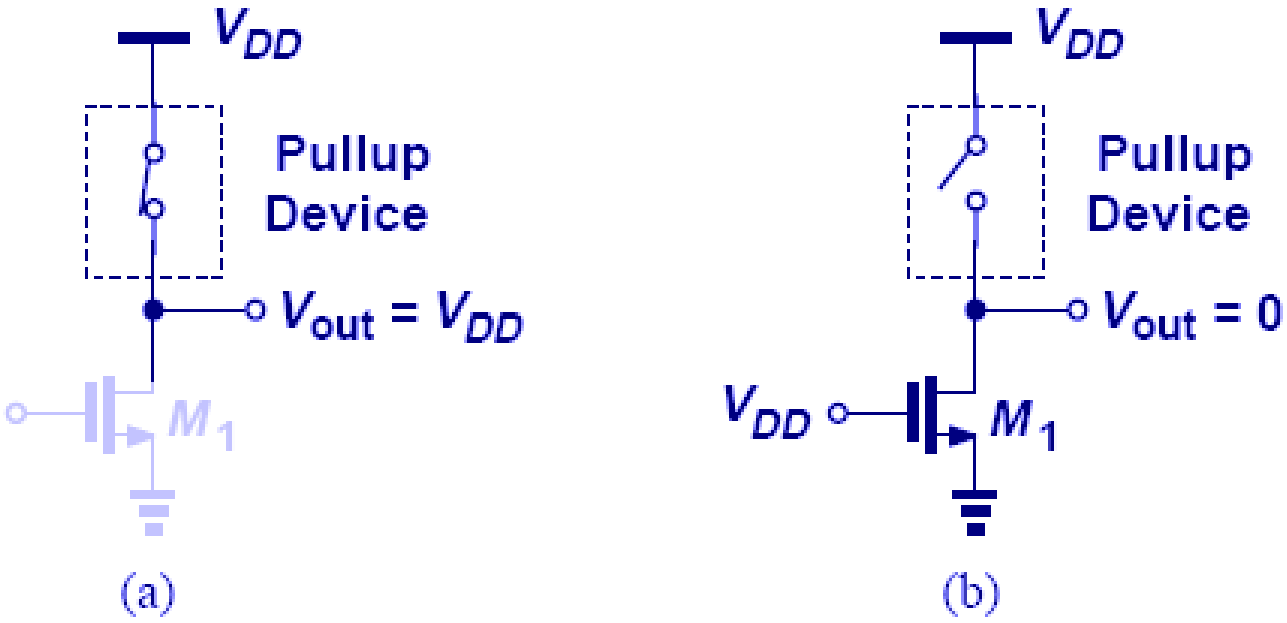
- **Noise margin is the amount of input logic level degradation that a gate can handle before the small-signal gain becomes -1.**

Drawbacks of the NMOS Inverter



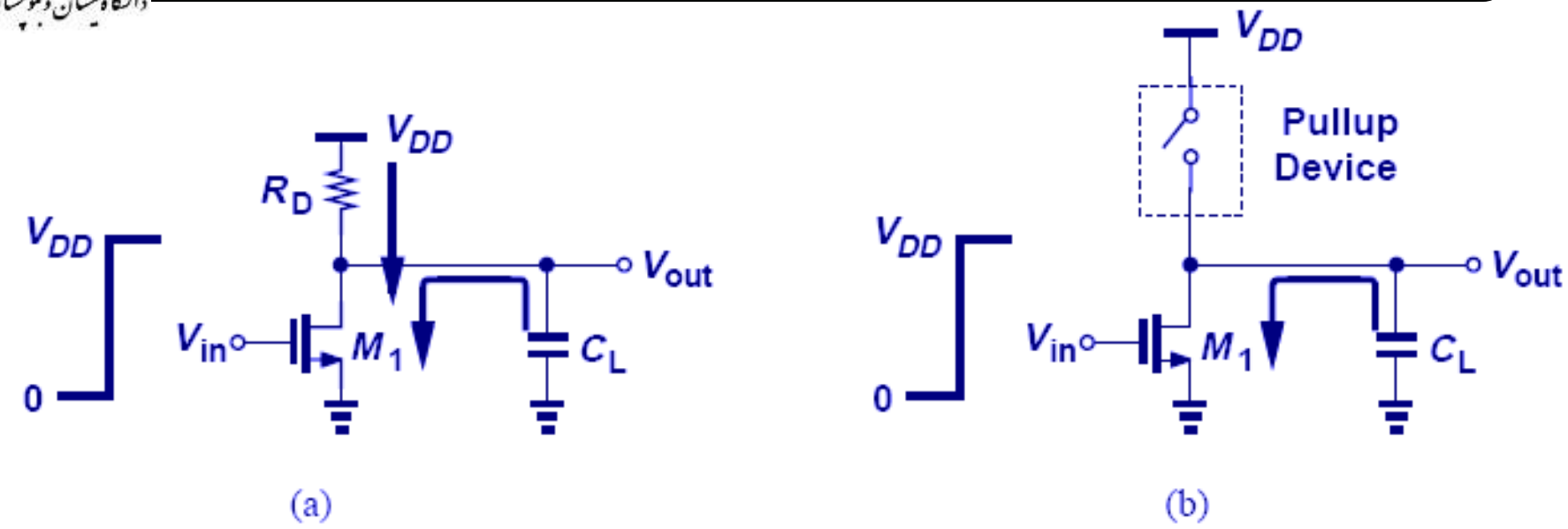
- Because of constant R_D, NMOS inverter consumes static power even when there is no switching.
- R_D presents a tradeoff between speed and power dissipation.

Improved Inverter Topology



- A better alternative would probably have been an "intelligent" pullup device that turns on when M_1 is off and vice versa.

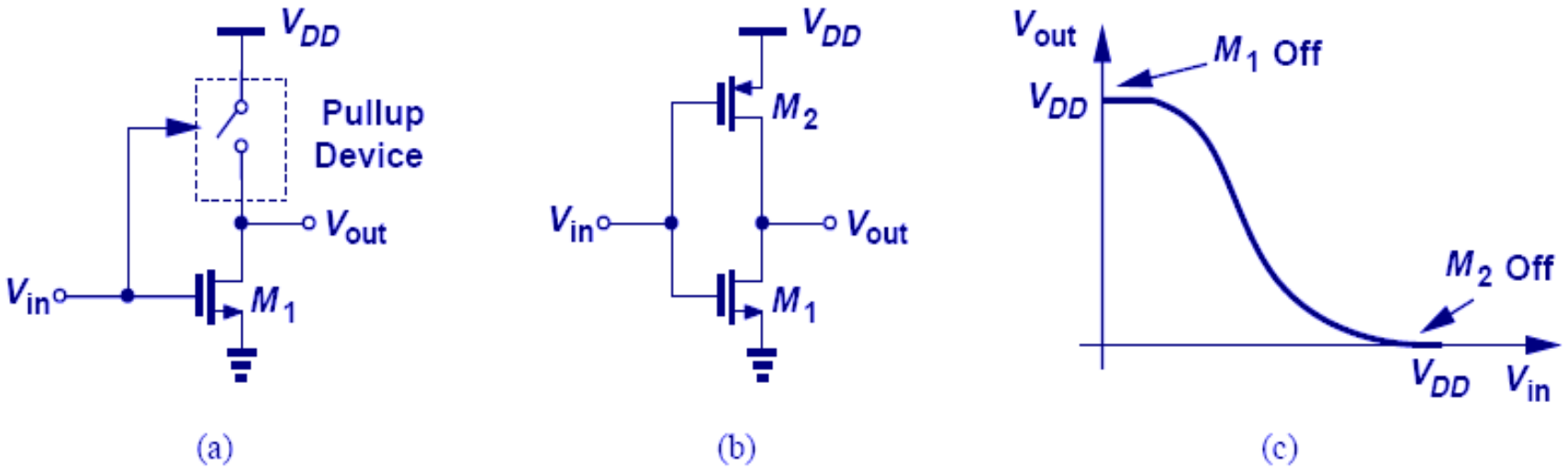
Improved Falltime



۱- برای عملکرد سوییچ، ترانزیستور حتما باید در ناحیه تریود قرار گیرد.
۲- ترانزیستور NMos دارای "1" ضعیف، ولی "0" خوب است.
(ترانزیستور PMOS برعکس.)

- **This improved inverter topology decreases falltime since all of the current from M_1 is available to discharge the capacitor.**

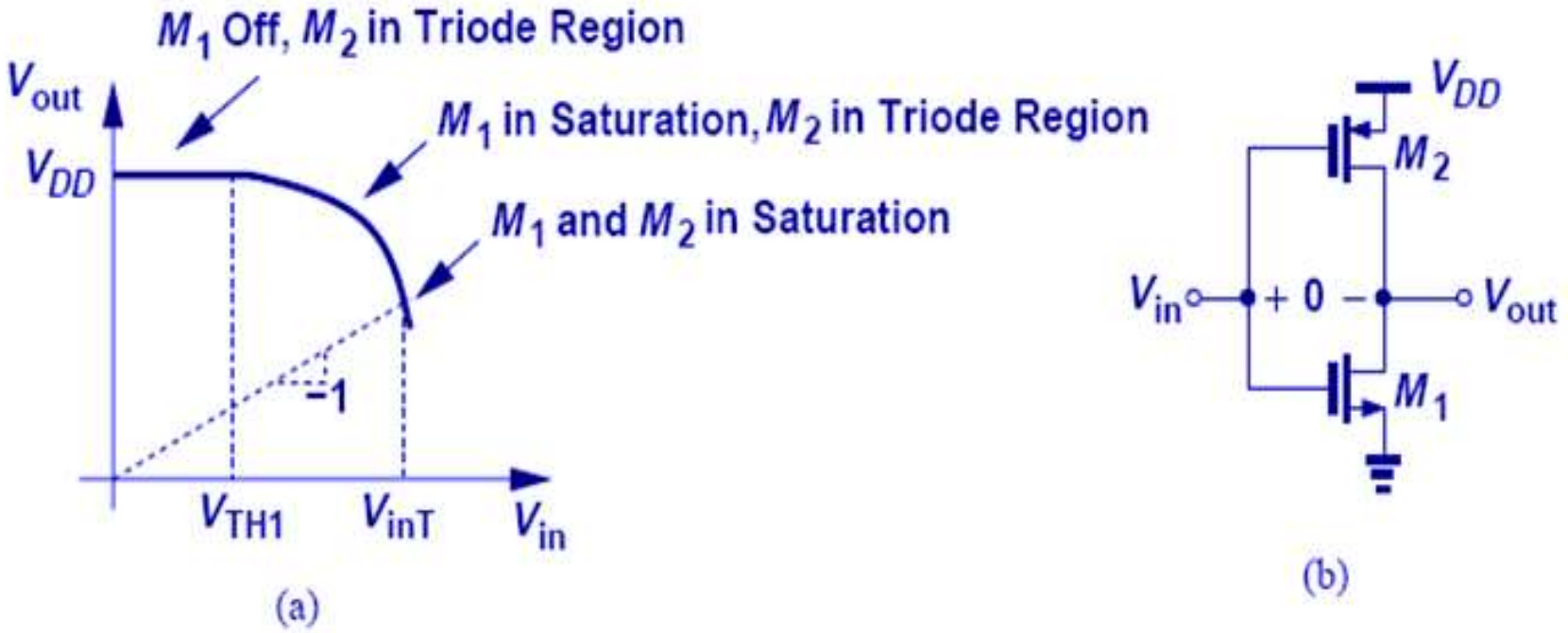
CMOS Inverter



۱- برای عملکرد سوییچ، ترانزیستور حتما باید در ناحیه تریود قرار گیرد.
۲- ترانزیستور NMos دارای "1" ضعیف، ولی "0" خوب است.
(ترانزیستور PMOS برعکس.)

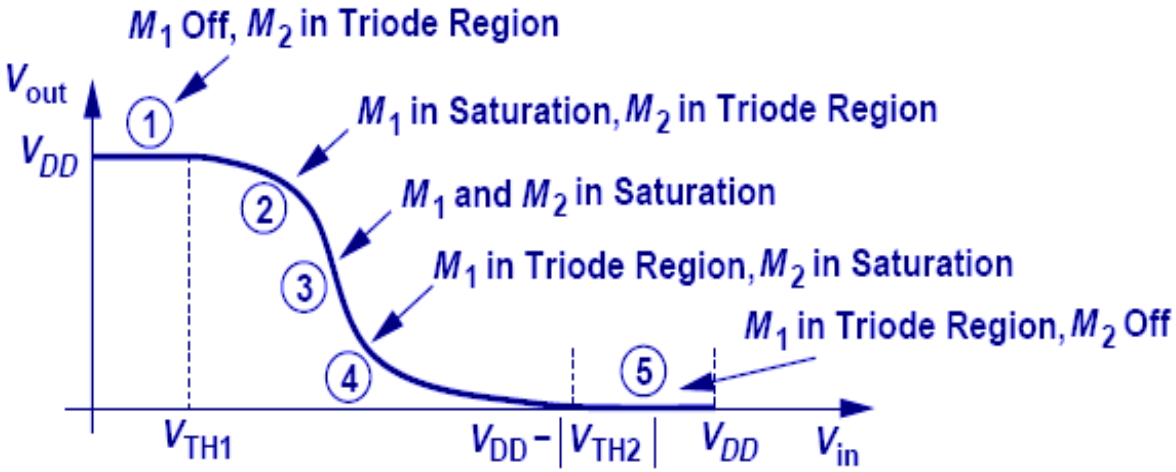
- **A circuit realization of this improved inverter topology is the CMOS inverter shown above.**
- **The NMOS/PMOS pair complement each other to produce the desired effects.**

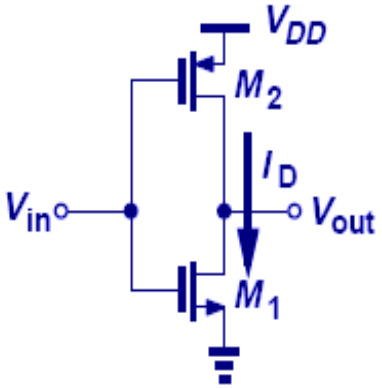
Switching Threshold



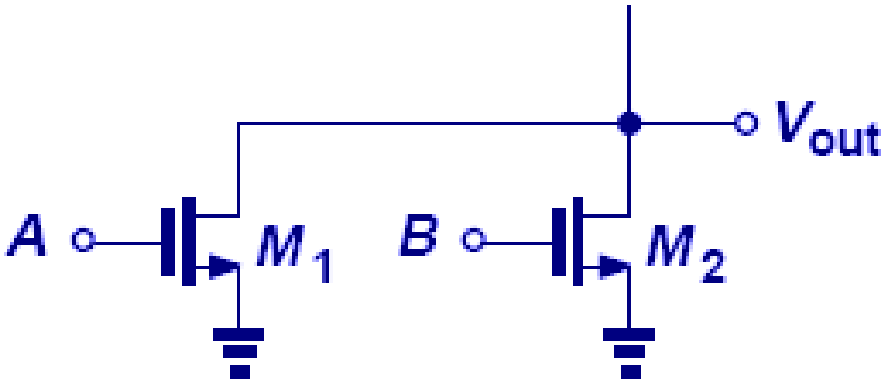
- The switching threshold (V_{inT}) or the "trip point" of the inverter is when V_{out} equals V_{in}.
- If $V_{inT} = V_{dd}/2$, then $W_2/W_1 = \mu_n/\mu_p$

CMOS Inverter VTC



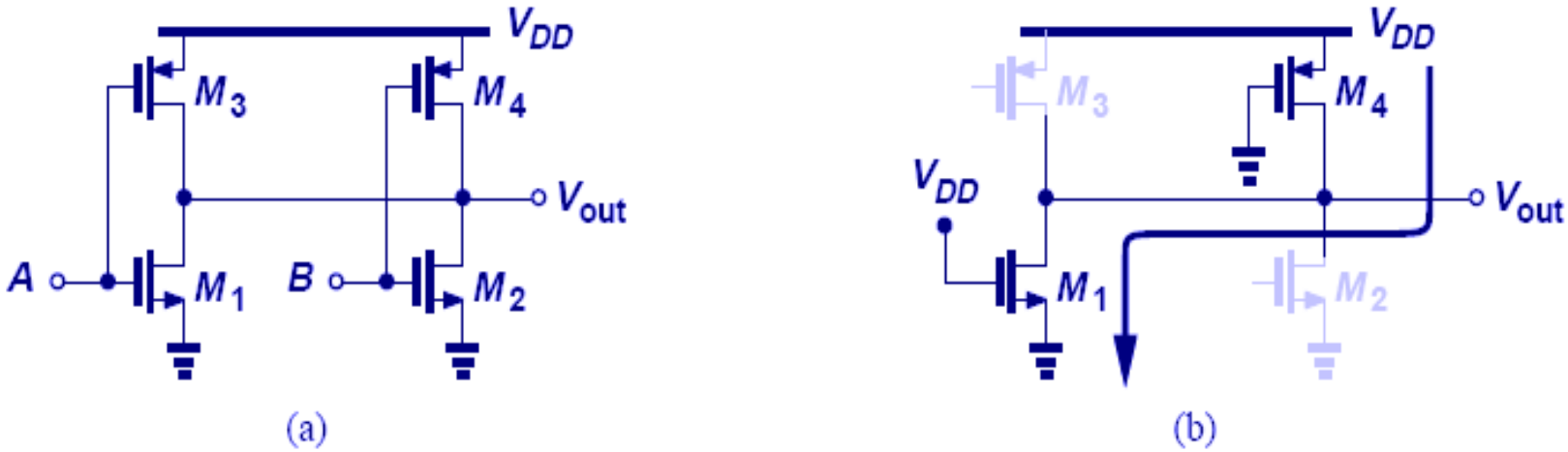


NMOS Section of NOR



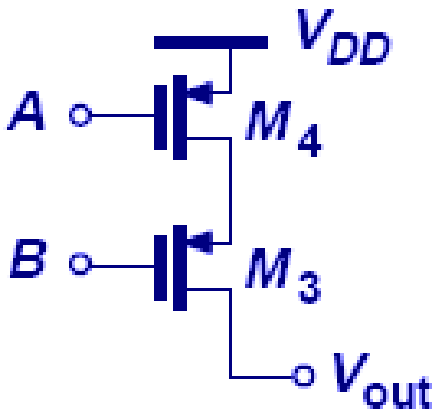
- **When either A or B is high or if both A and B are high, the output will be low. Transistors operate as pull-down devices.**

Example: Poor NOR



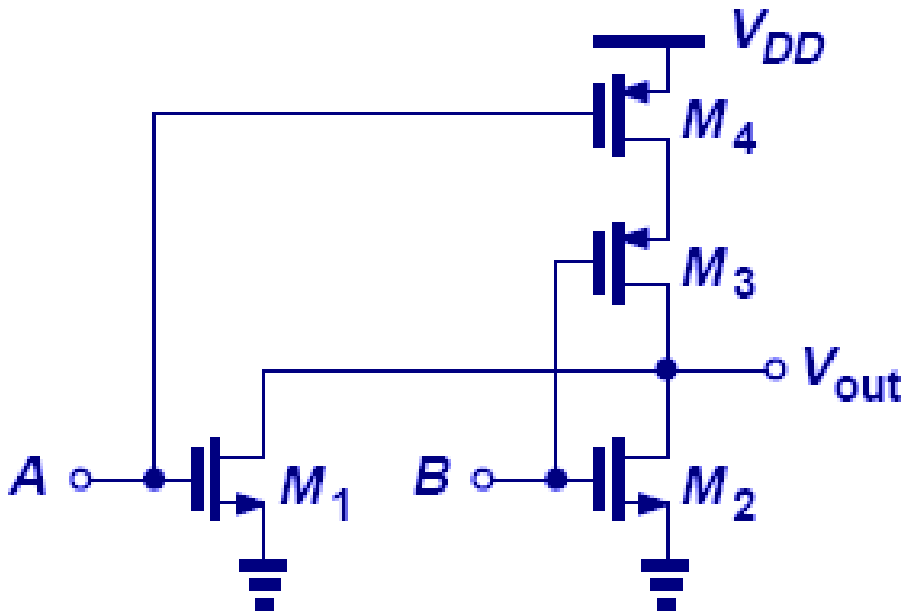
- **The above circuit fails to act as a NOR because when A is high and B is low, both M_4 and M_1 are on and produces an ill-defined low.**

PMOS Section of NOR



- **When both A and B are low, the output is high. Transistors operate as pull-up devices.**

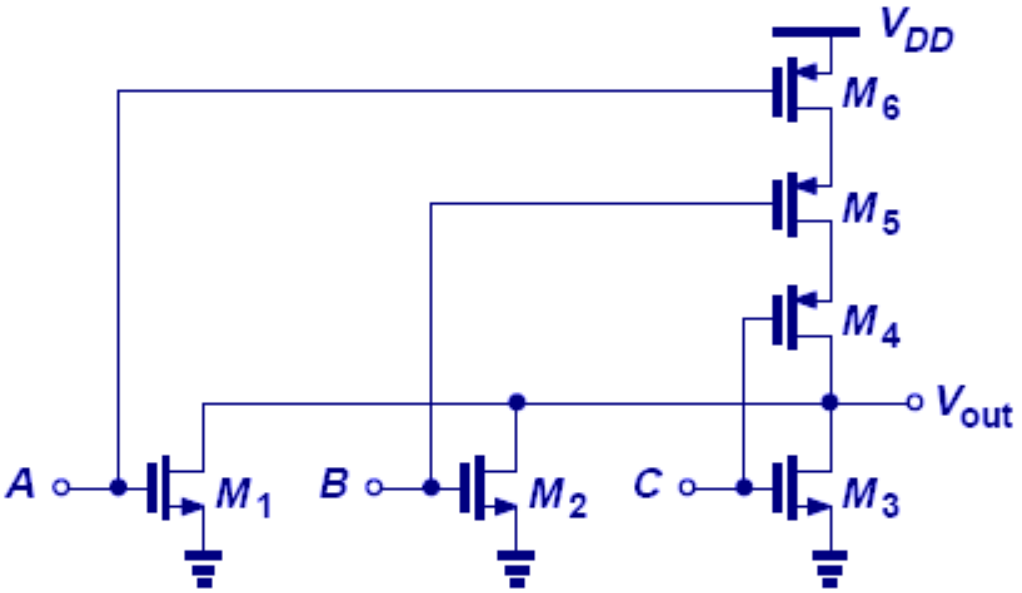
CMOS NOR



$$Vout=\overline{(A+B)}$$

- **Combing the NMOS and PMOS NOR sections, we have the CMOS NOR.**

Example: Three-Input NOR



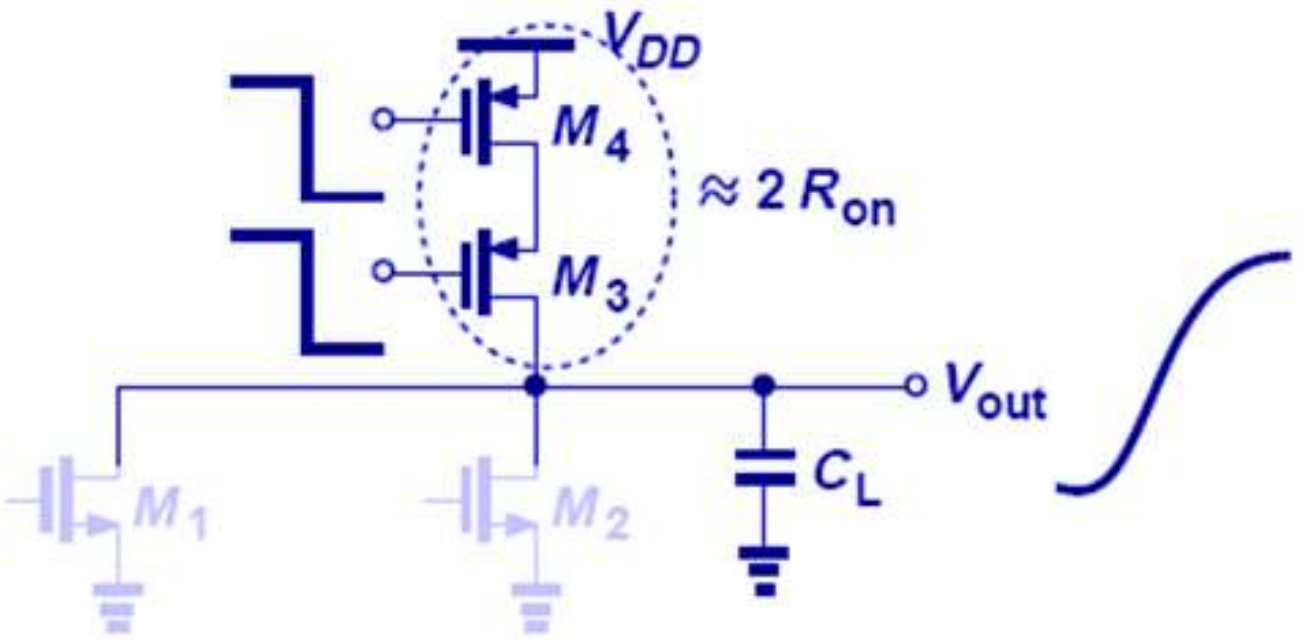
$$V_{out} = \left(A + B + C\right)'$$

Equal Rise & Fall ($\mu_n \approx 2\mu_p$)

$W_1=W_2=W_3=W$

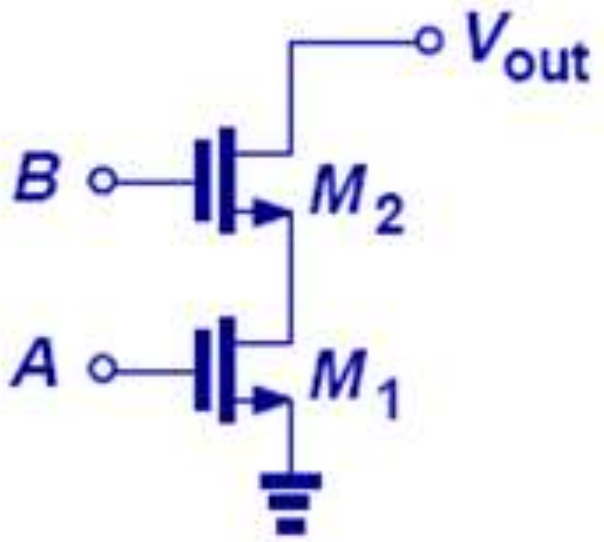
$W_4=W_5=W_6=6W$

Drawback of CMOS NOR



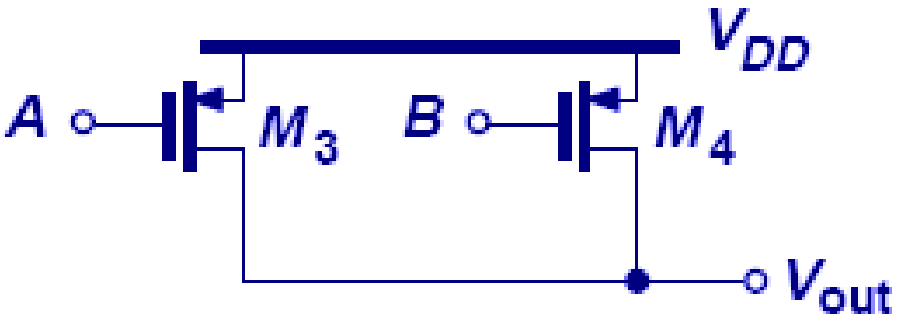
- **Due to low PMOS mobility, series combination of M_3 and M_4 suffers from a high resistance, producing a long delay.**
- **The widths of the PMOS transistors can be increased to counter the high resistance, however this would load the preceding stage and the overall delay of the system may not improve.**

NMOS NAND Section



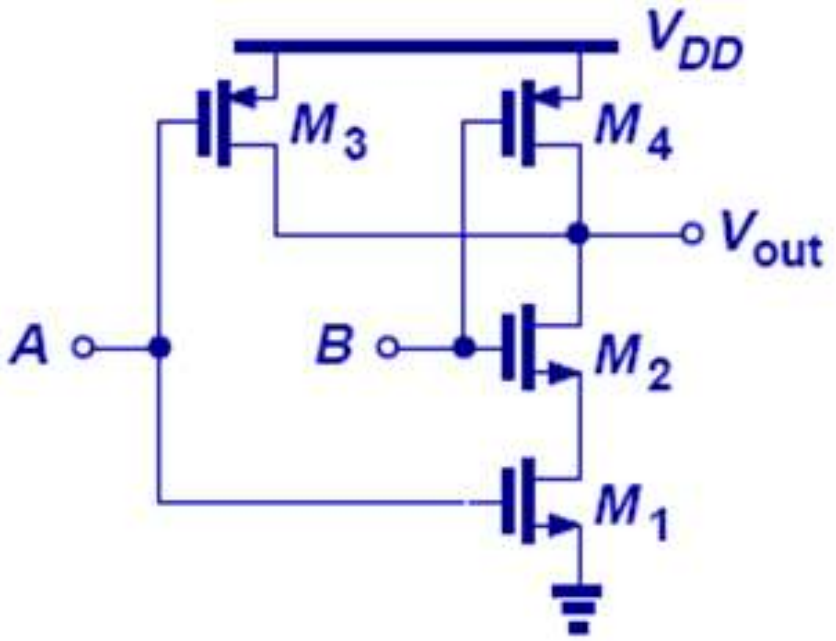
- **When both A and B are high, the output is low.**

PMOS NOR Section



- **When either A or B is low or if both A and B are low, the output is high.**

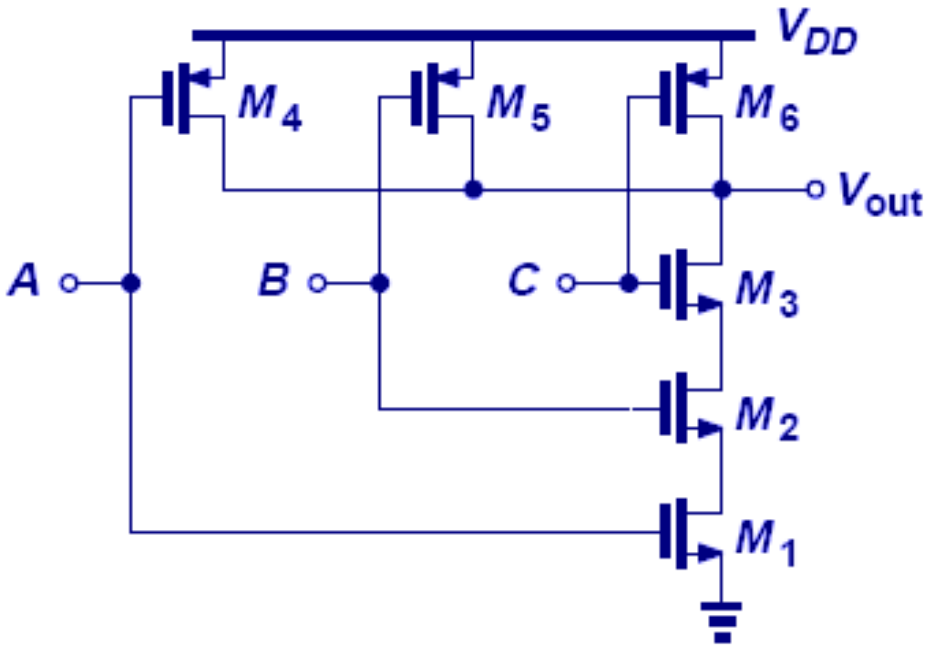
CMOS NAND



$$Vout=\overline{(A.B)}$$

- **Just like the CMOS NOR, the CMOS NAND can be implemented by combining its respective NMOS and PMOS sections, however it has better performance because its PMOS transistors are not in series.**

Example: Three-Input NAND



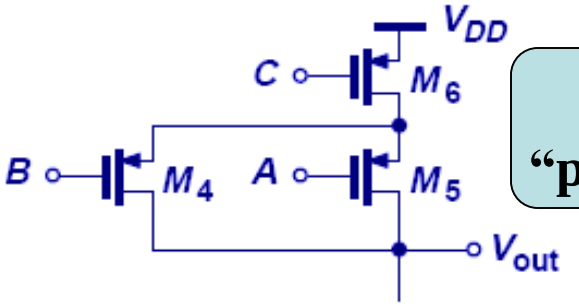
$$V_{out} = (ABC)'$$

Equal Rise & Fall ($\mu_n \approx 2\mu_p$)

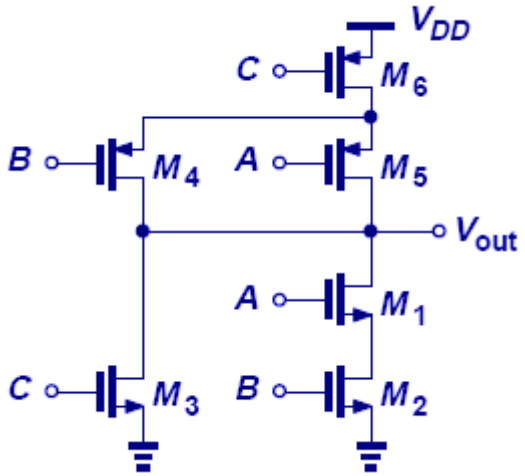
$W_1=W_2=W_3=3W$

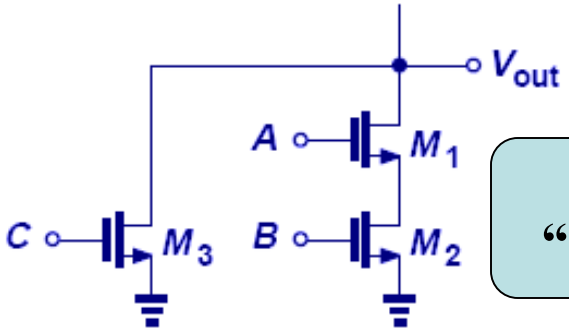
$W_4=W_5=W_6=2W$

NMOS and PMOS Duality



C is in "series" with the "parallel" combination of A and B





C is in "parallel" with the "series" combination of A and B

- **In the CMOS philosophy, the PMOS section can be obtained from the NMOS section by converting series combinations to the parallel combinations and vice versa.**