



فصل ۱۰ - تقویت کننده های تفاضلی

(قسمت سوم - زوج تفاضلی با بار فعال)

Mohammad Ali Mansouri- Birjandi

Majid Ghadrdan

Faculty of Electrical and Computer Engineering
University of Sistan and Baluchestan (USB)

mansouri@ece.usb.ac.ir ,
mamansouri@yahoo.com



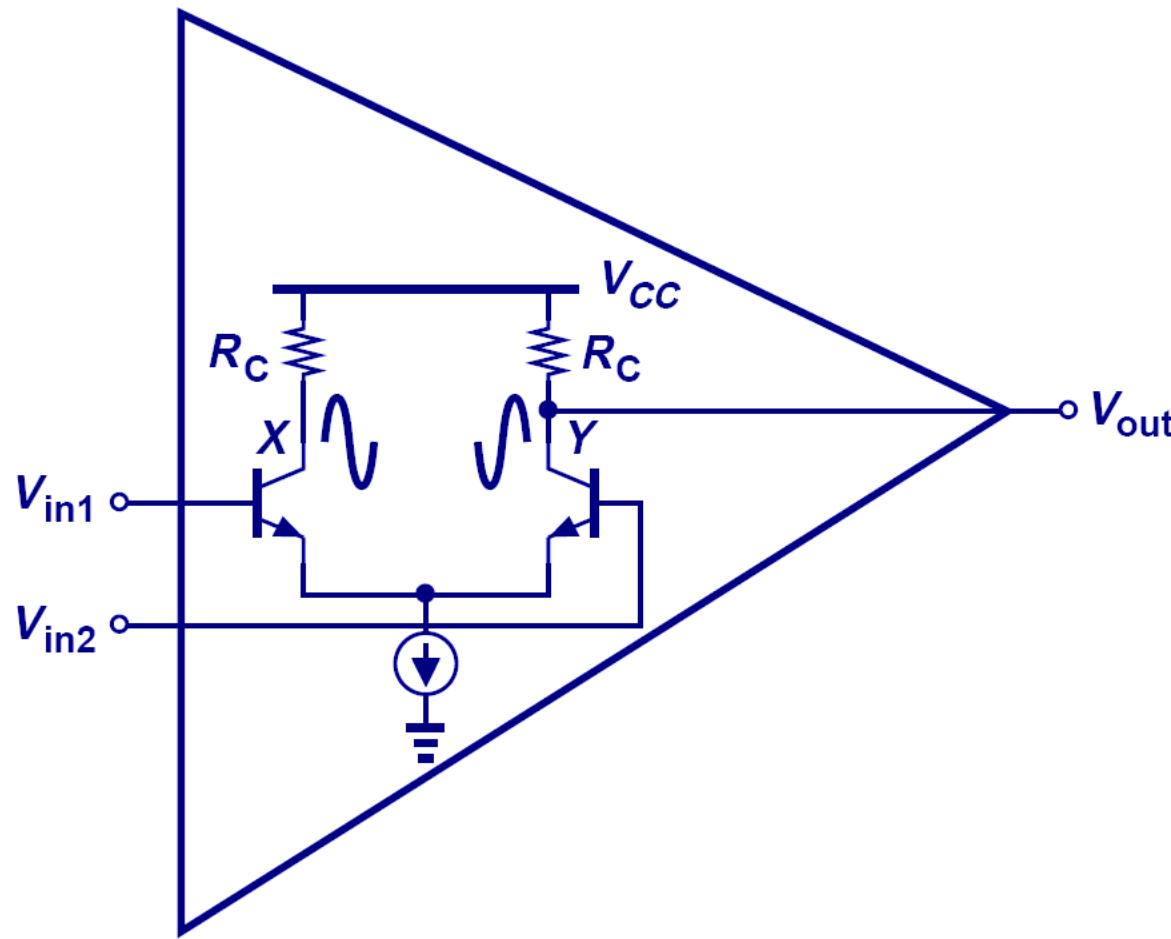
Chapter 10 Differential Amplifiers

➤ 10.6 Differential Pair with Active Load



Differential to Single-ended Conversion

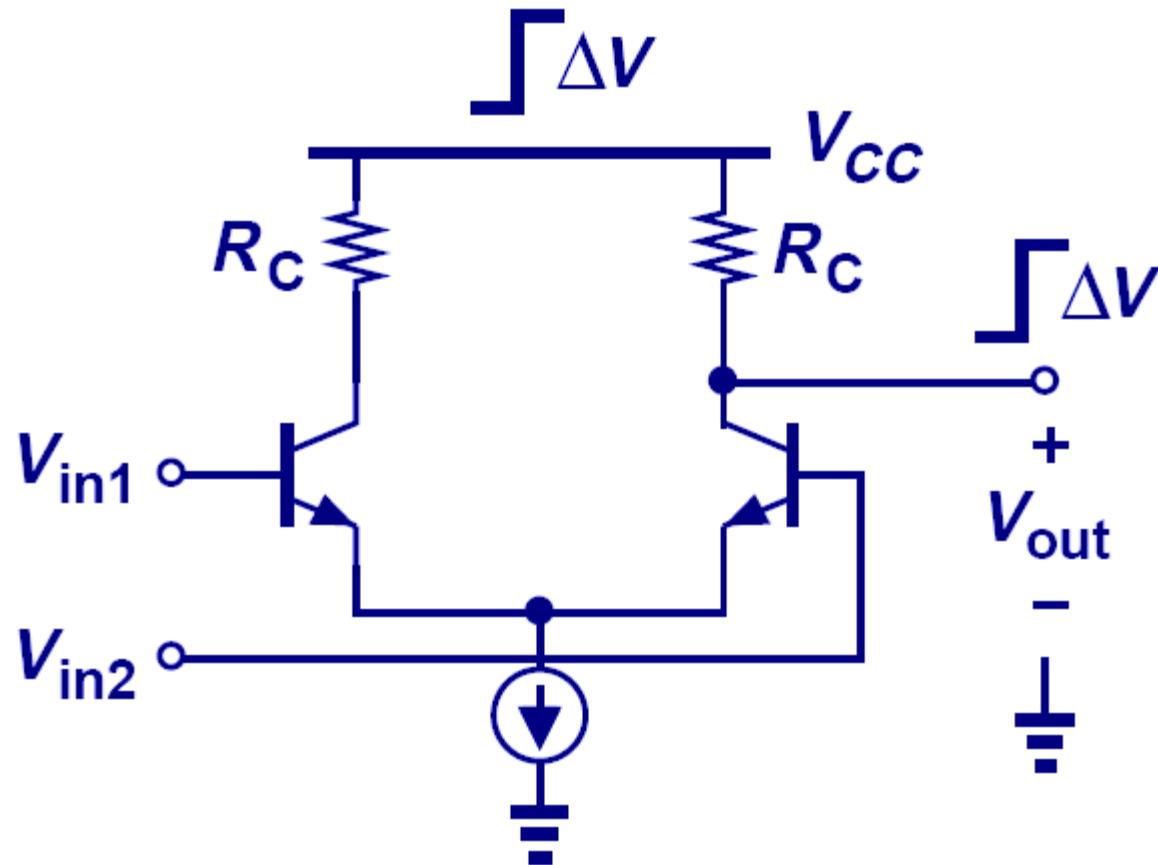
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- Many circuits require a differential to single-ended conversion, however, the above topology is not very good.



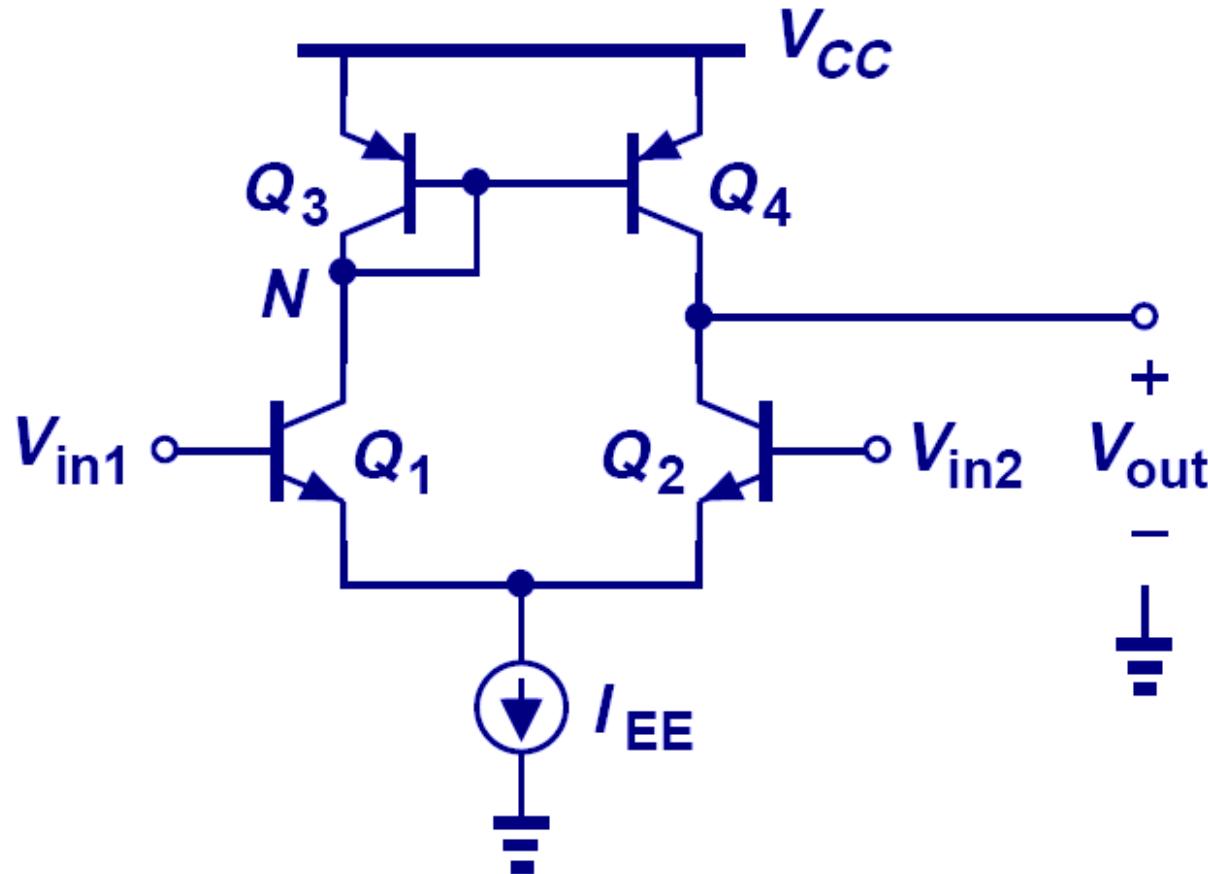
Supply Noise Corruption



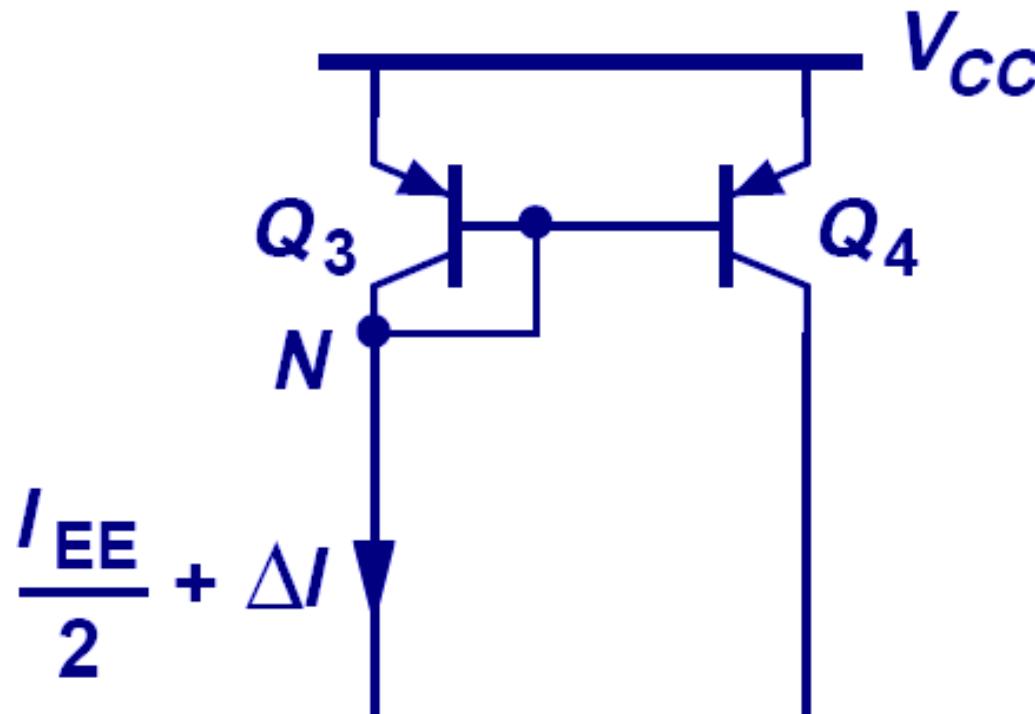
- The most critical drawback of this topology is supply noise corruption, since no common-mode cancellation mechanism exists. Also, we lose half of the signal.



Better Alternative



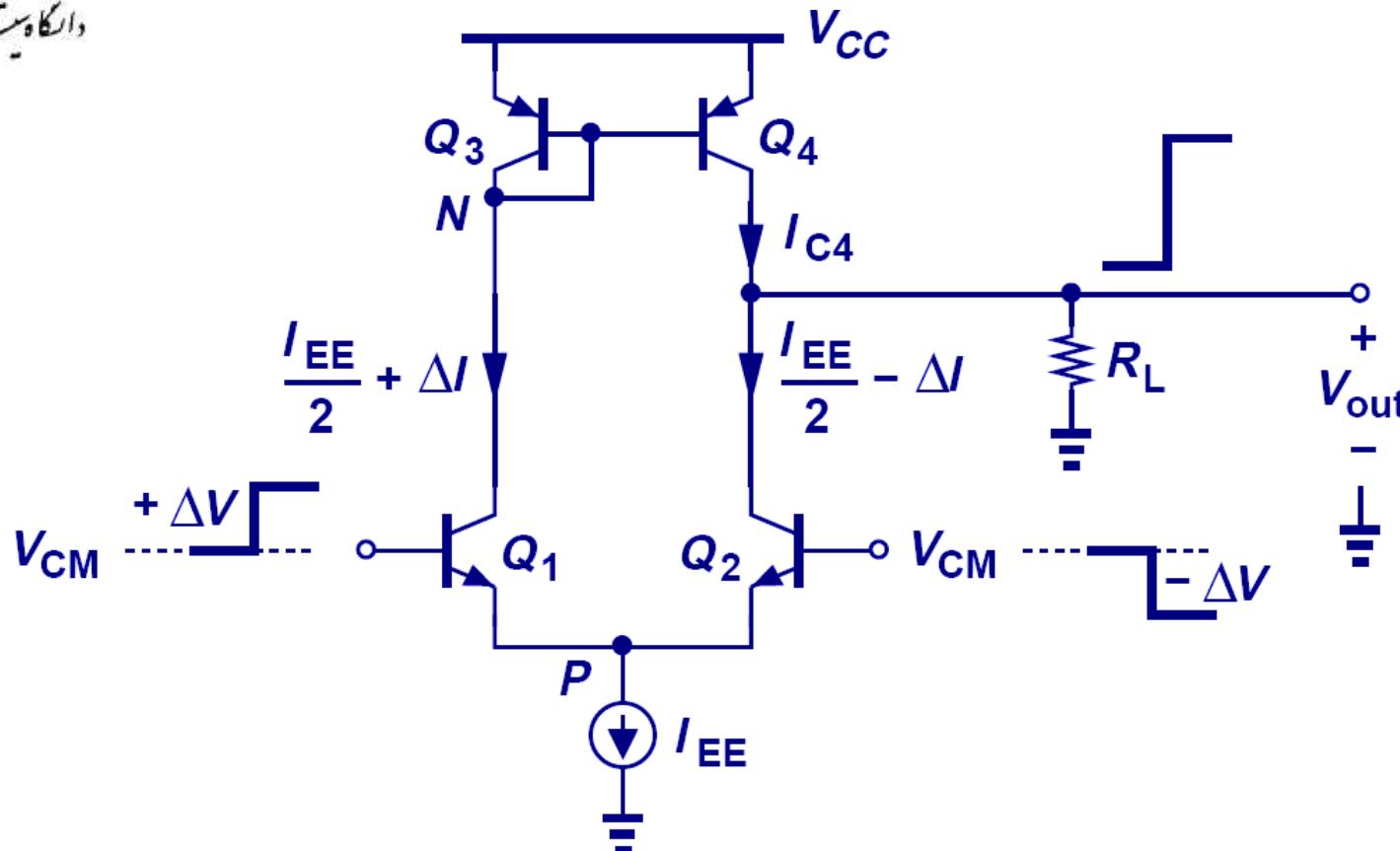
- This circuit topology performs differential to single-ended conversion with no loss of gain.



- With current mirror used as the load, the signal current produced by the Q_1 can be replicated onto Q_4 .
- This type of load is different from the conventional “static load” and is known as an “active load”.



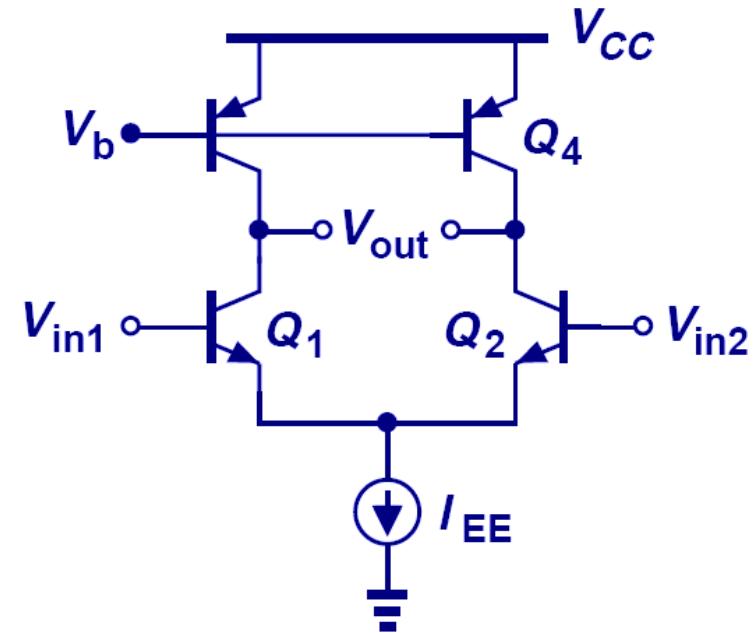
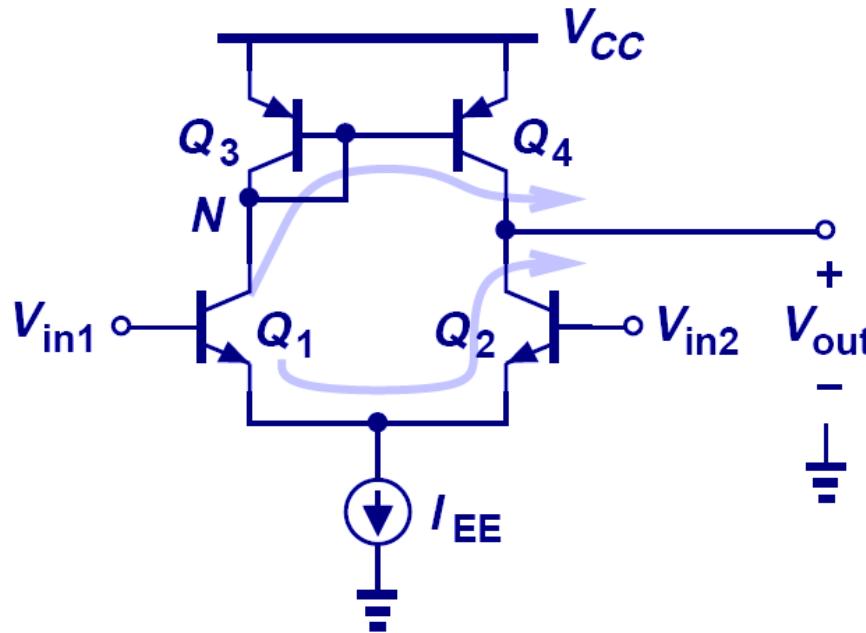
Differential Pair with Active Load



- The input differential pair decreases the current drawn from R_L by ΔI and the active load pushes an extra ΔI into R_L by current mirror action; these effects enhance each other.



Active Load vs. Static Load

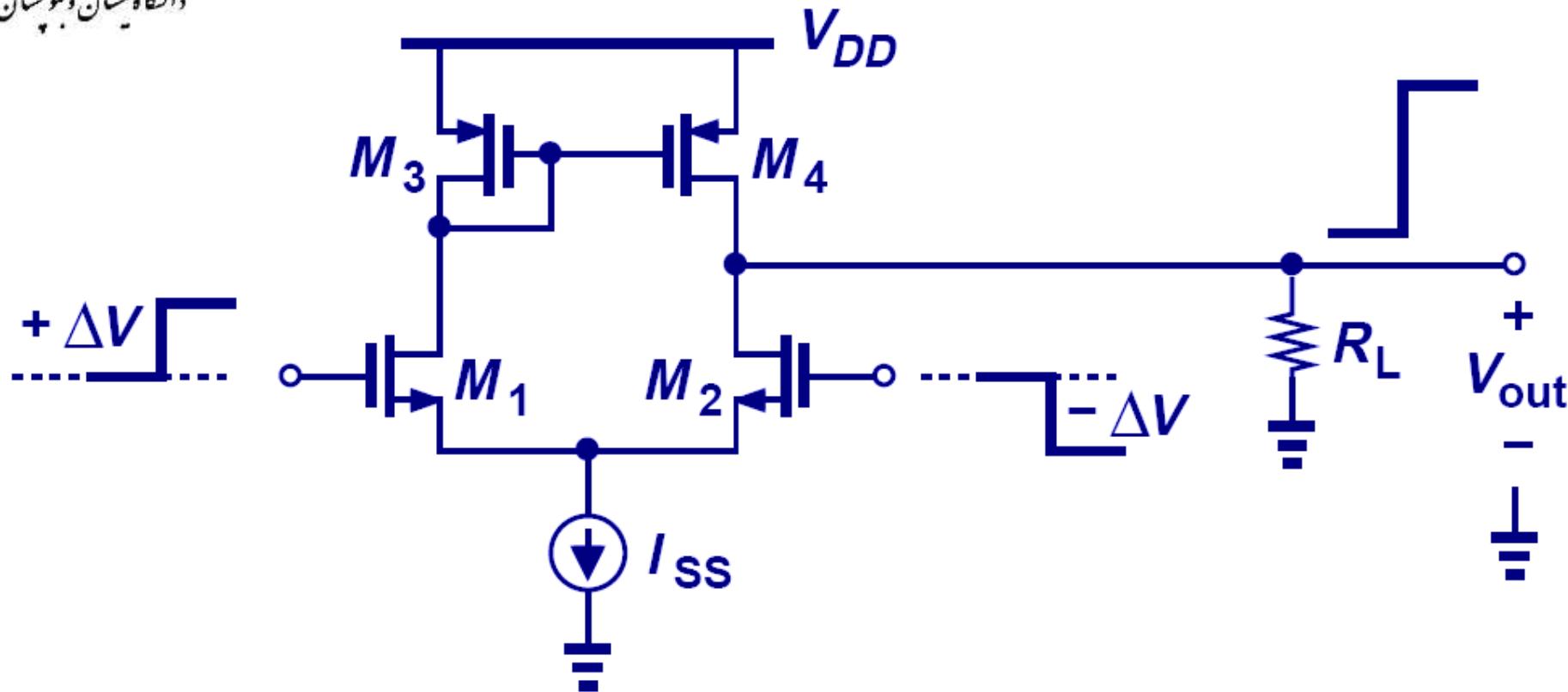


- The load on the left responds to the input signal and enhances the single-ended output, whereas the load on the right does not.



MOS Differential Pair with Active Load

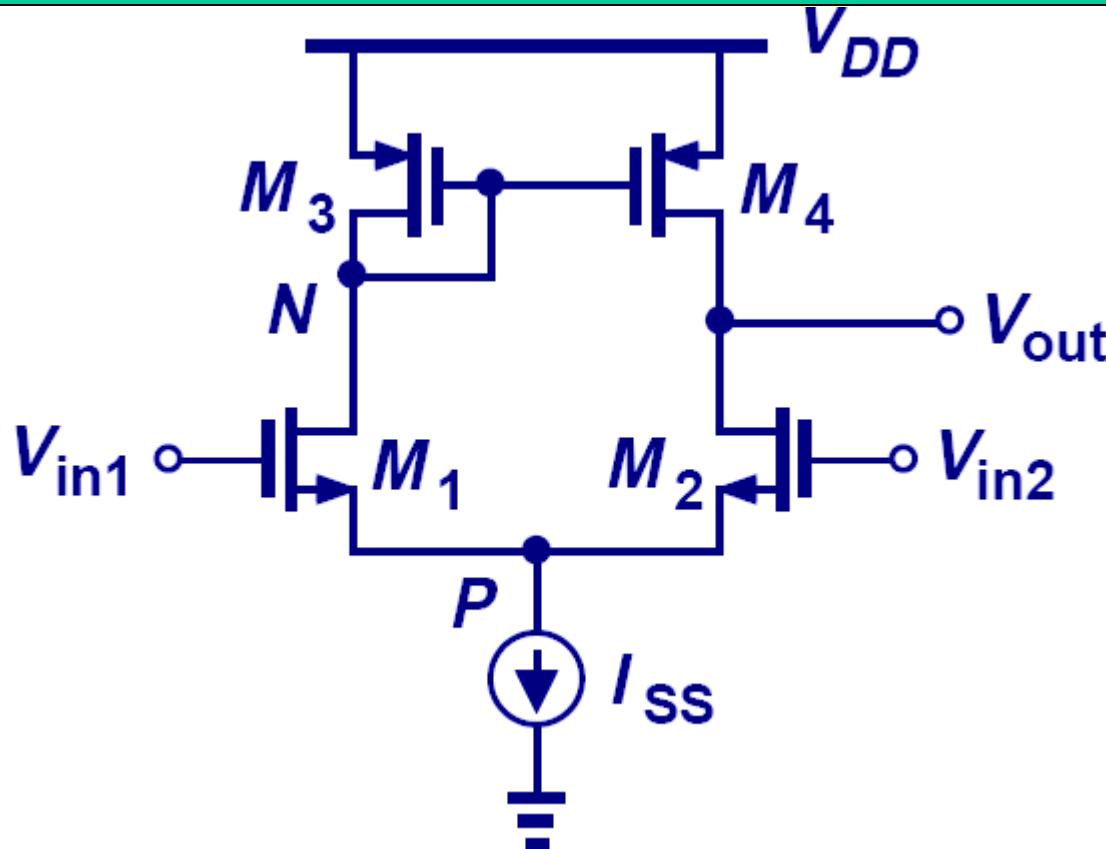
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- Similar to its bipolar counterpart, MOS differential pair can also use active load to enhance its single-ended output.



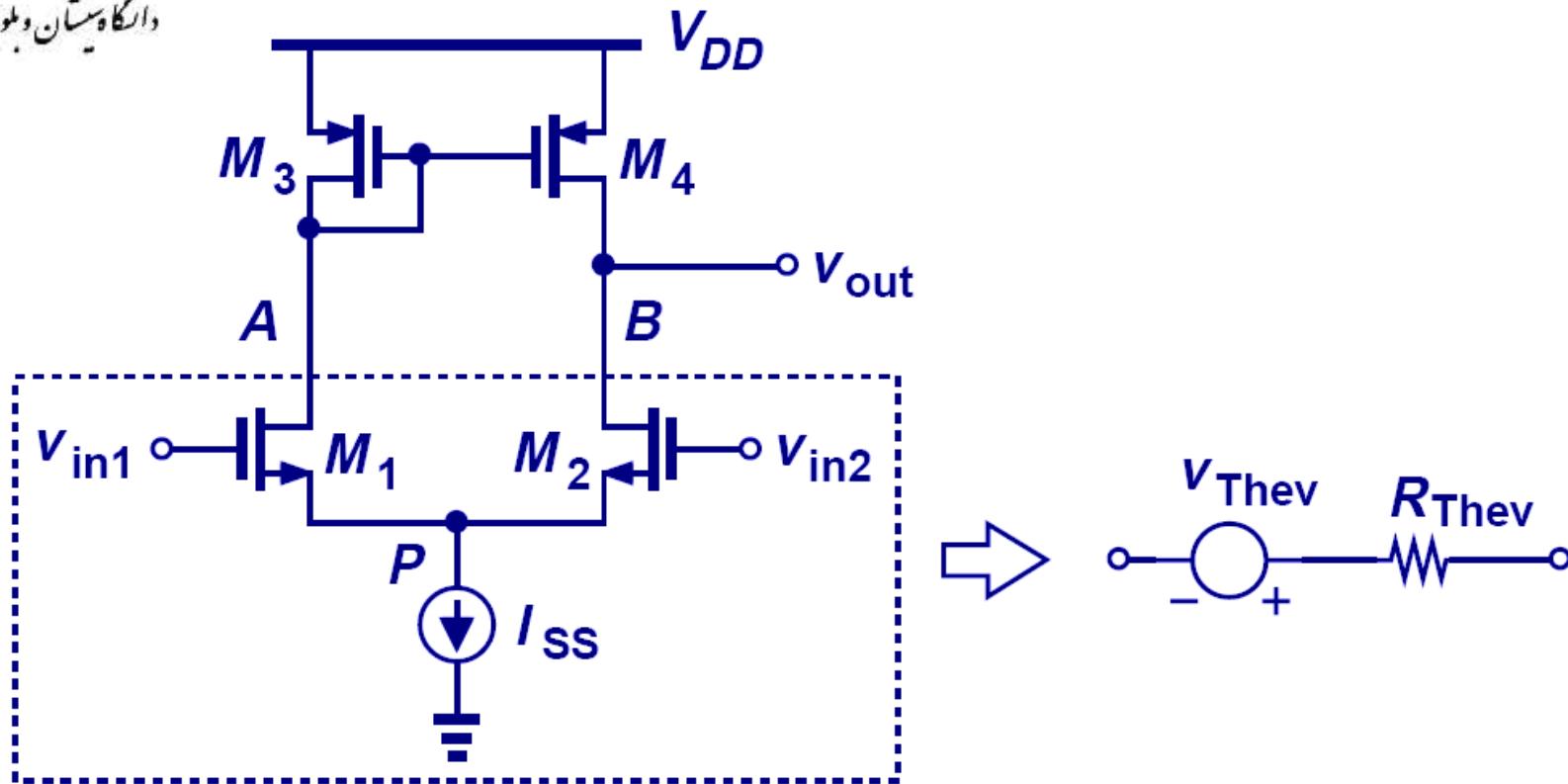
Asymmetric Differential Pair



- Because of the vastly different resistance magnitude at the drains of M_1 and M_2 , the voltage swings at these two nodes are different and therefore node P cannot be viewed as a virtual ground.



Thevenin Equivalent of the Input Pair



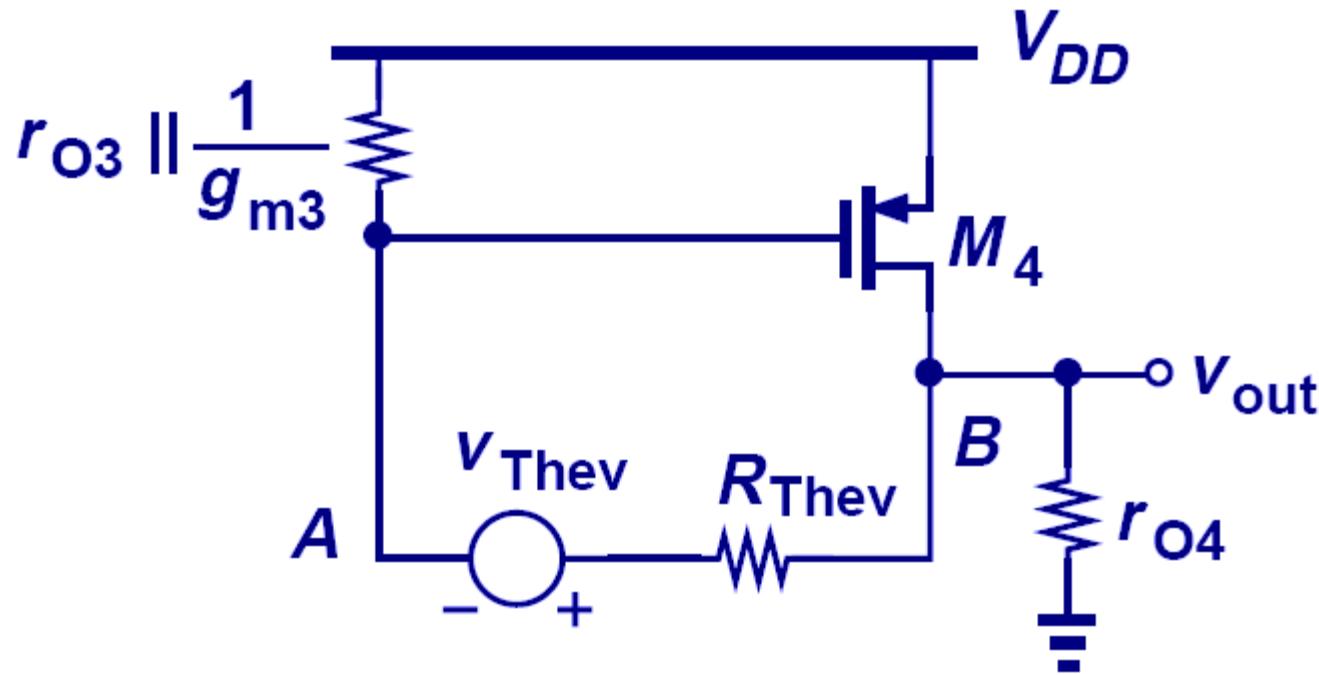
$$v_{Thev} = -g_{mN} r_{oN} (v_{in1} - v_{in2})$$

$$R_{Thev} = 2r_{oN}$$



Simplified Differential Pair with Active Load

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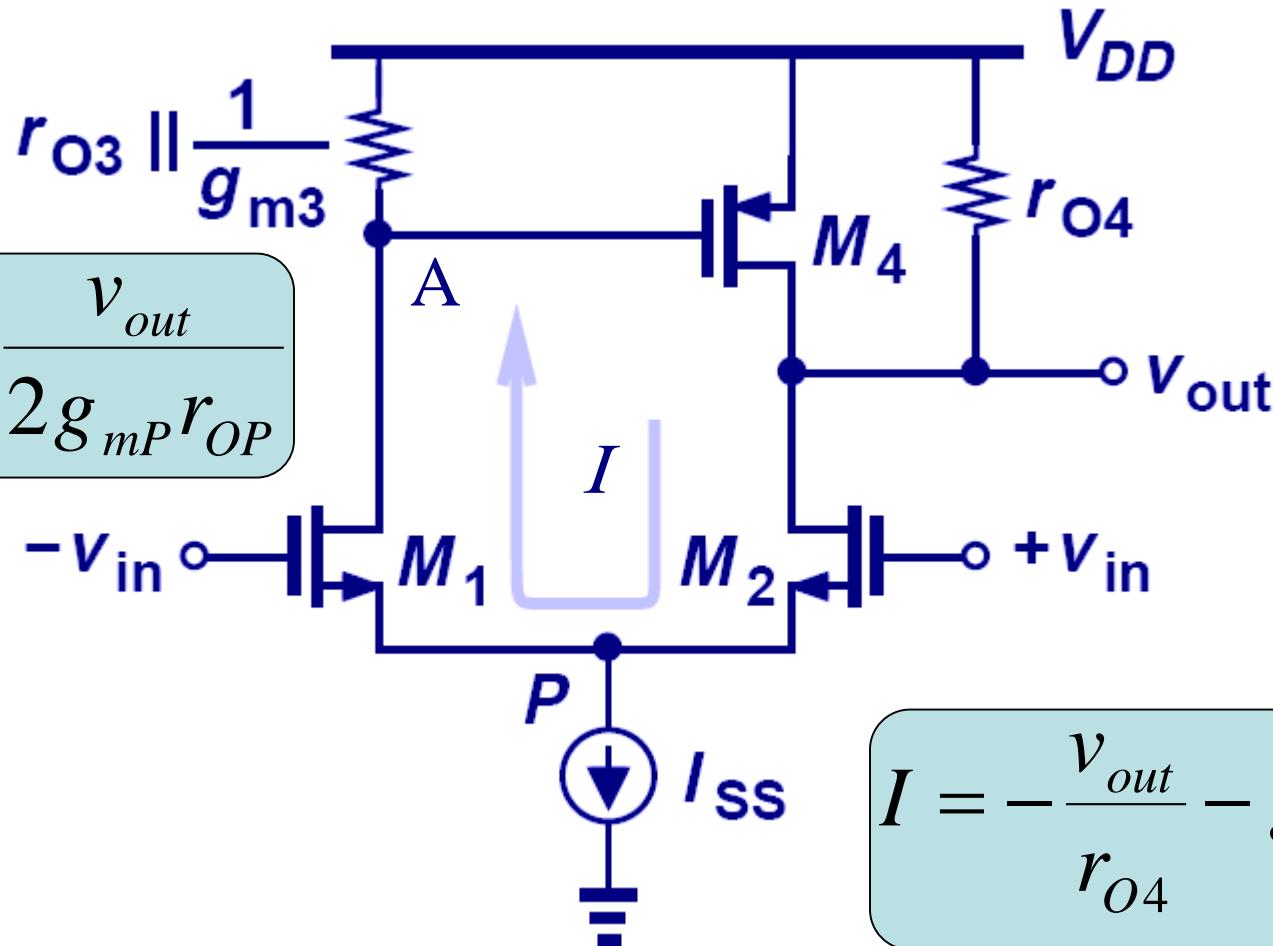


$$\frac{v_{out}}{v_{in1} - v_{in2}} = g_{mN} (r_{ON} \parallel r_{OP})$$

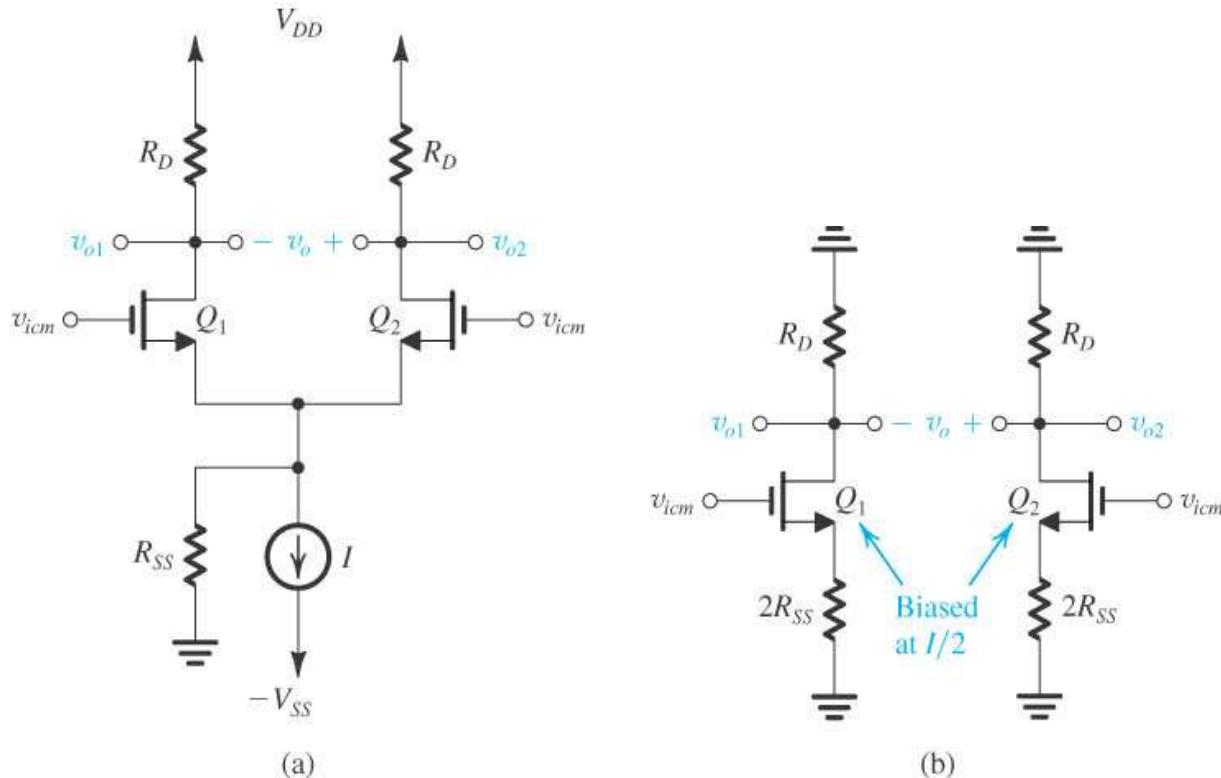


Proof of $V_A \ll V_{out}$

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Common-mode input signal

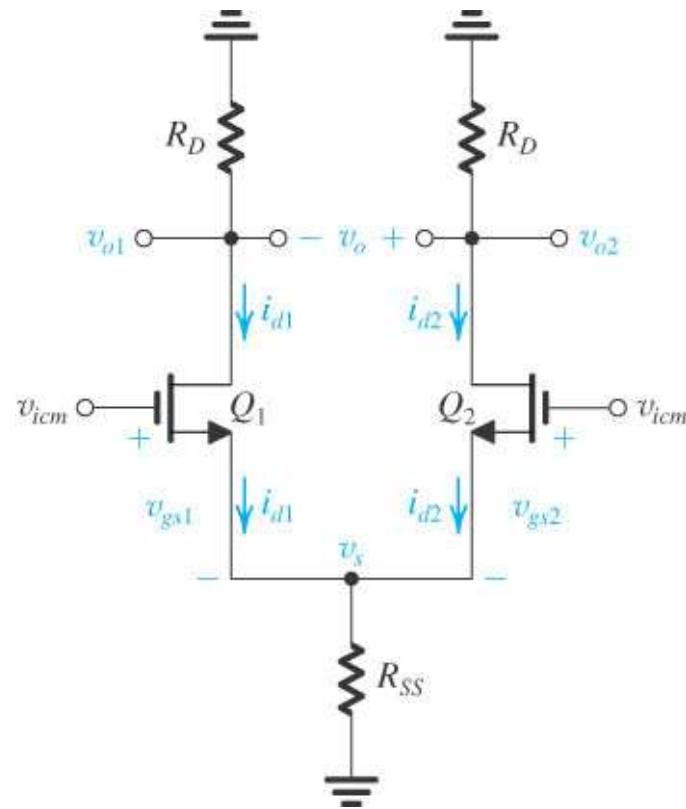


(a) The MOS differential amplifier with a common-mode input signal v_{icm}

(b) Equivalent circuit for determining the common-mode gain (with r_o ignored).

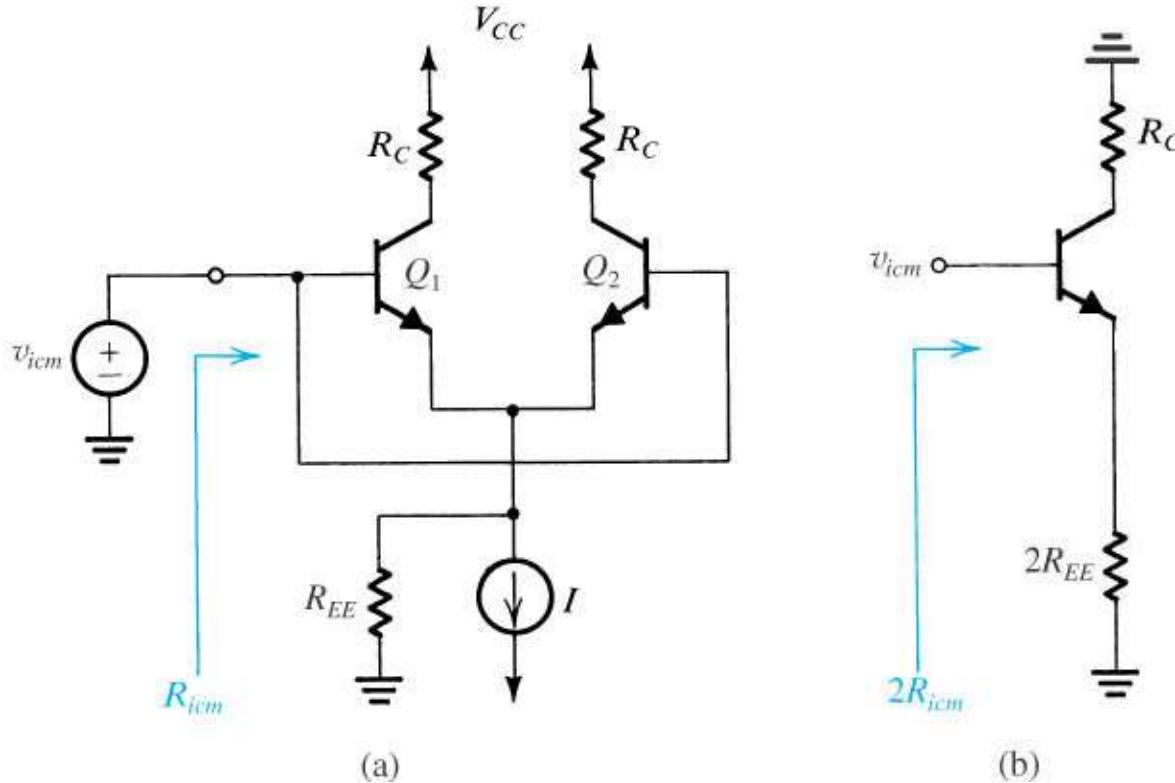
Each half of the circuit is known as the “**common-mode half-circuit**.”

Common-Mode Gain

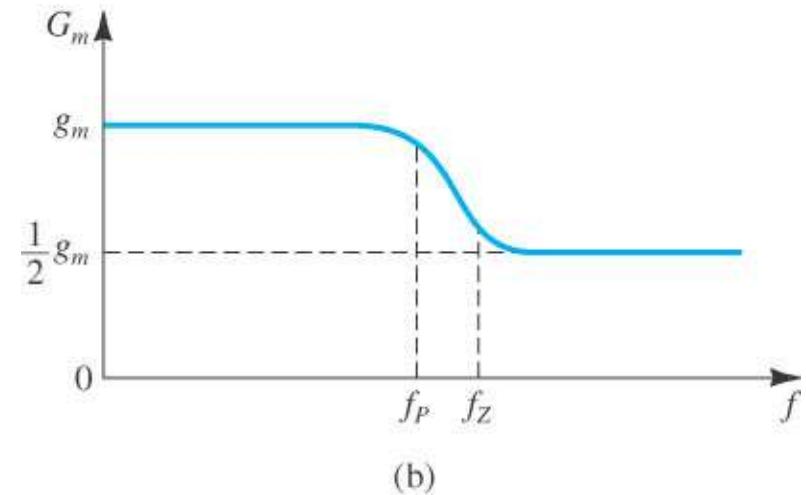
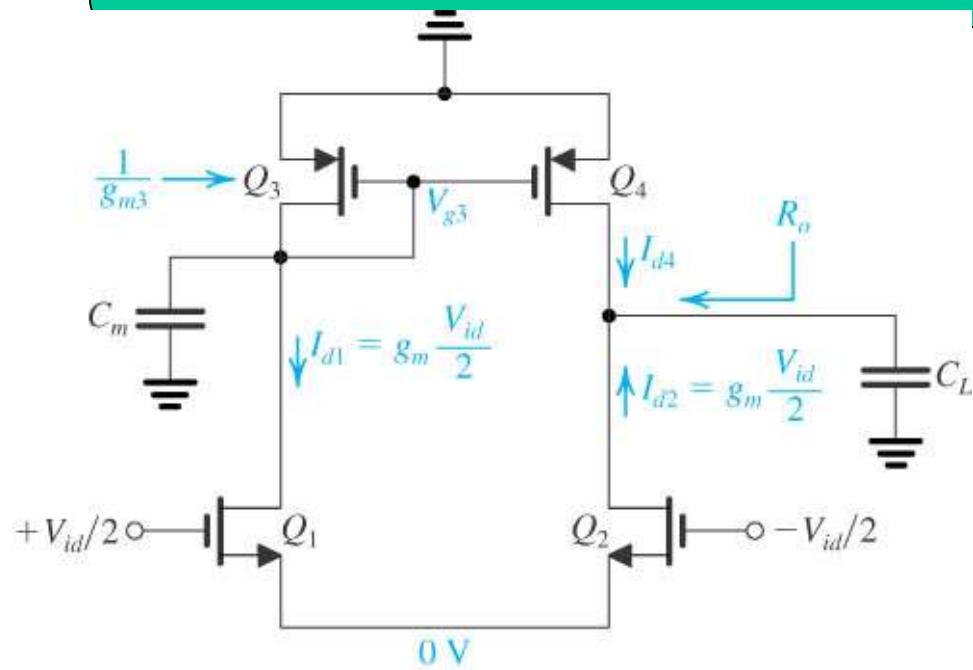


Analysis of the MOS differential amplifier to determine the common-mode gain resulting from a mismatch in the g_m values of Q_1 and Q_2 .

input common-mode resistance R_{icm}



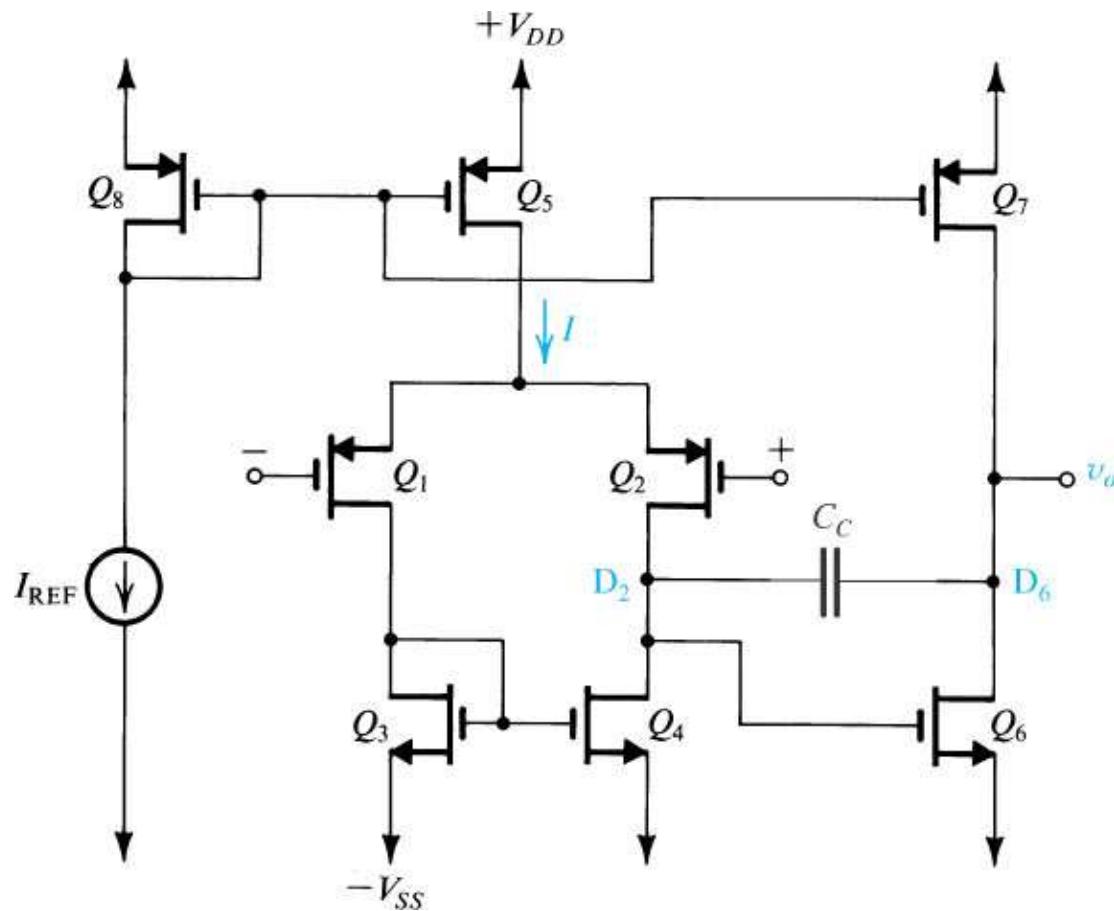
- (a) Definition of the input common-mode resistance R_{icm} .
- (b) The equivalent common-mode half-circuit.



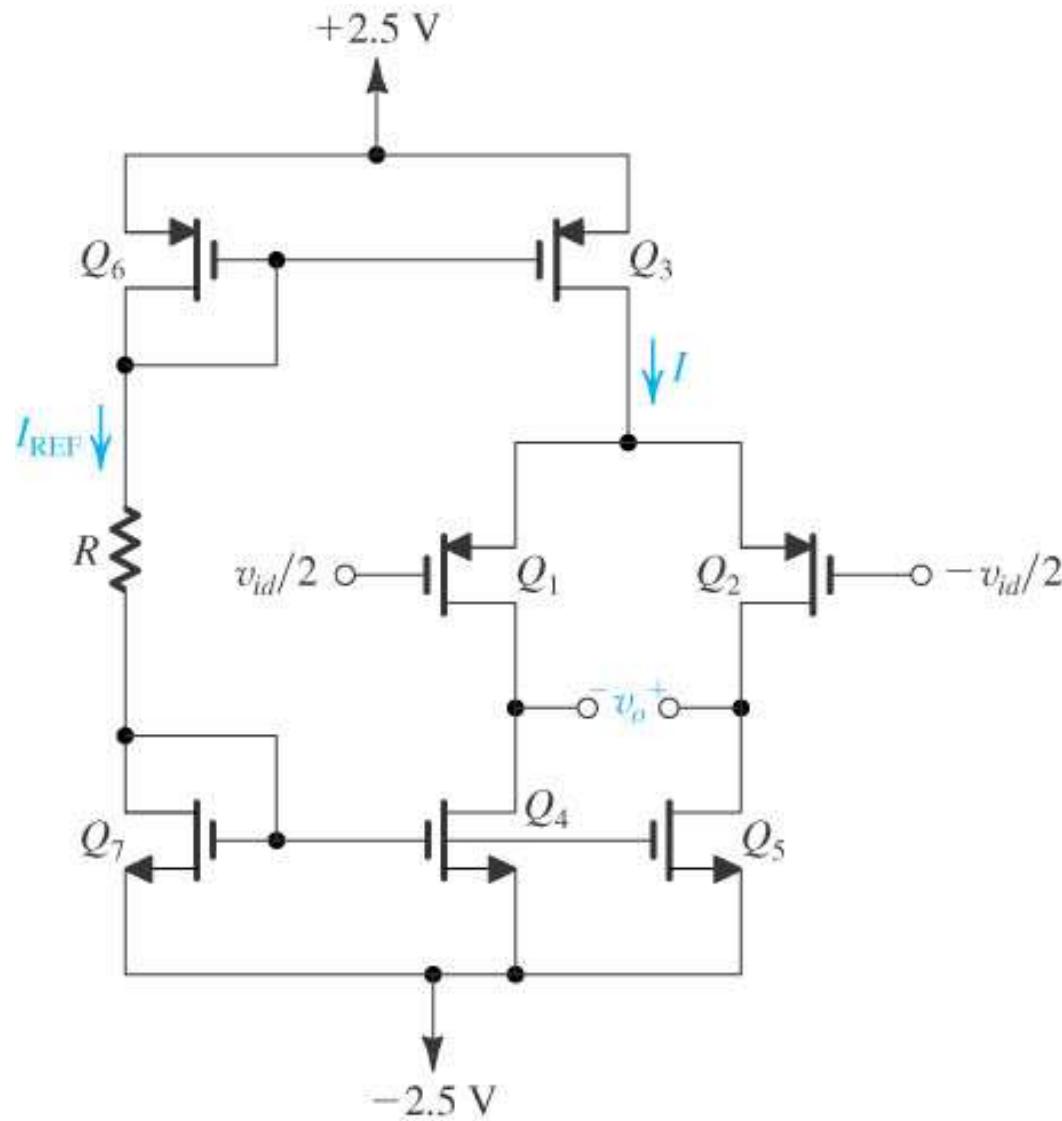
(a) Frequency-response analysis of the active-loaded MOS differential amplifier.

(b) The overall transconductance G_m as a function of frequency.

Two-stage CMOS op-amp configuration.



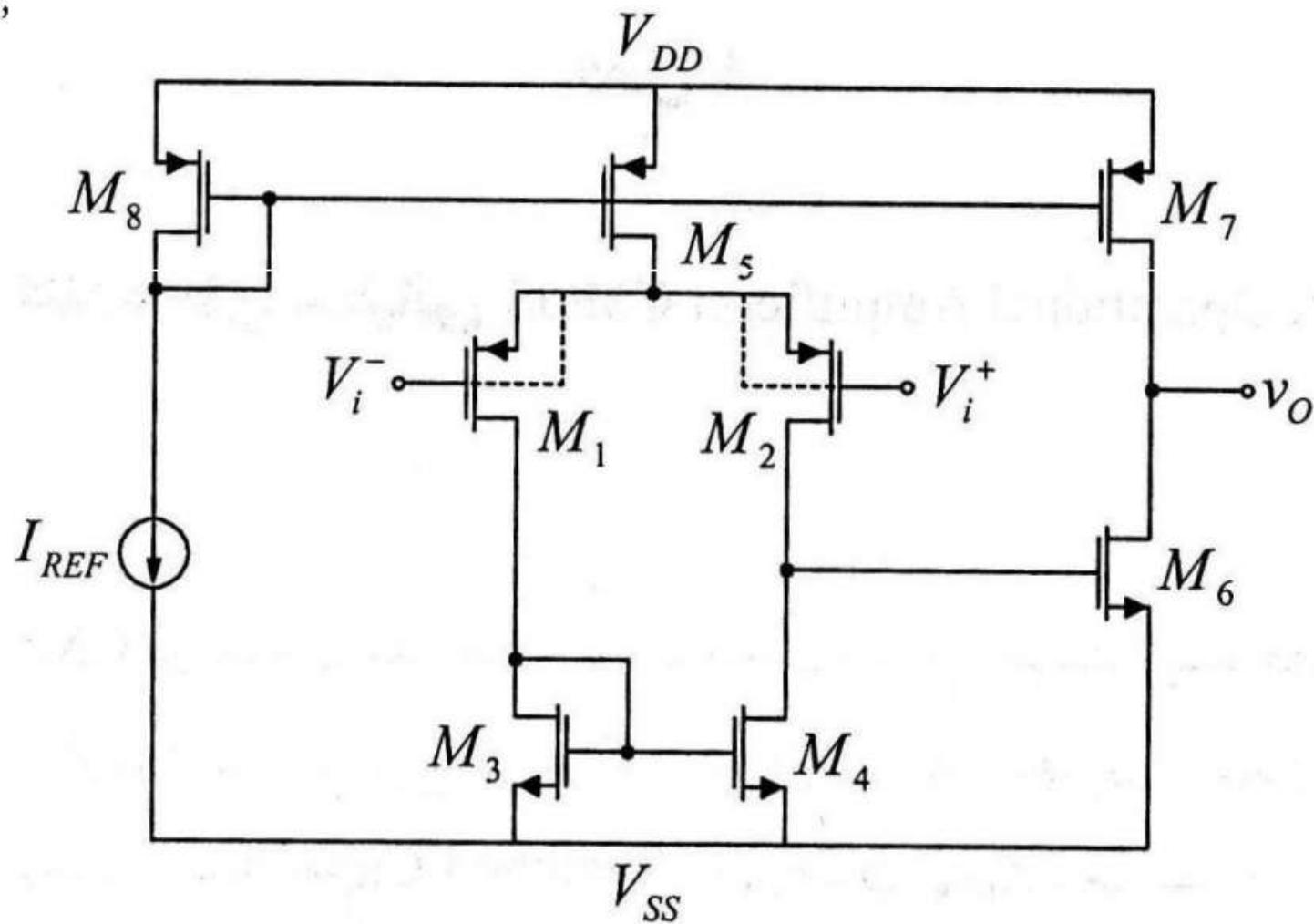
MOS Differential Amplifier





MOS Differential Amplifier

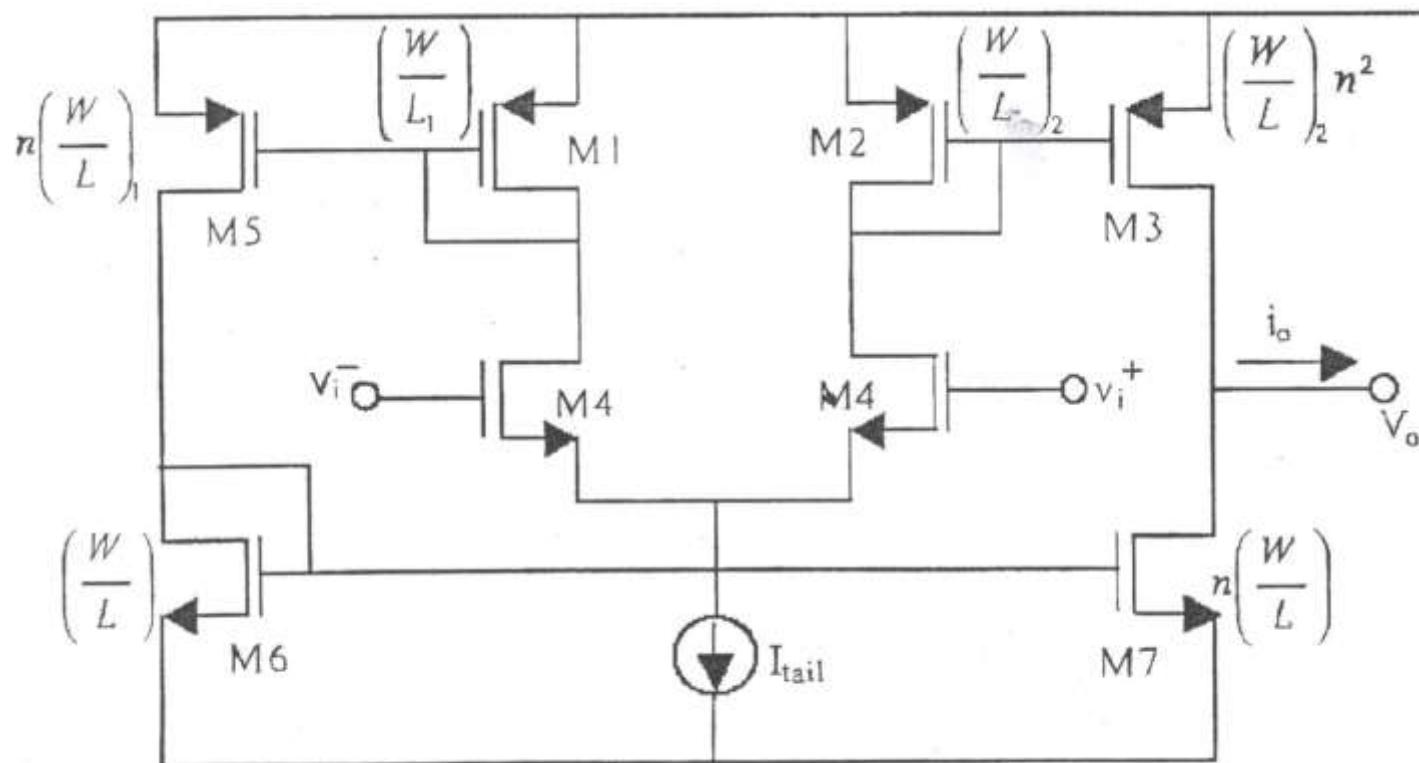
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Example: $G_m = ?$

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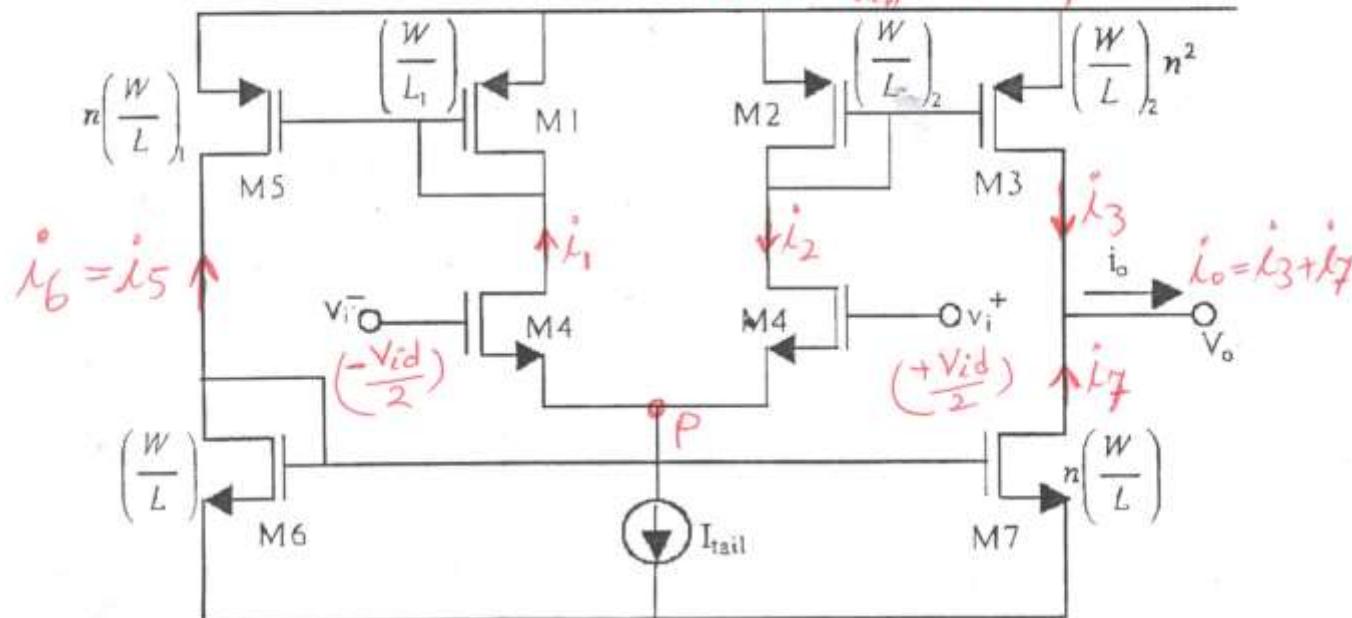


Example: $G_m = ?$

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$$i_o = i_3 + i_7 = 2n^2 i_1 = 2n^2 \left(g_{m4} \frac{V_{id}}{2} \right) = n^2 g_{m4} V_{in}$$

$$G_m \triangleq \frac{i_o}{V_{in}} = n^2 g_{m4}$$



$$i_1 = g_{m4} \left(\frac{V_{id}}{2} \right)$$

$$i_2 = g_{m4} \left(\frac{V_{id}}{2} \right)$$

$$i_3 = n^2 i_2 = n^2 i_1$$

$$i_5 = i_6 = n i_1$$

$$i_7 = n i_5 = n^2 i_1$$

نیز i_1, i_2 نیز
(i_5, i_6 نیز)

